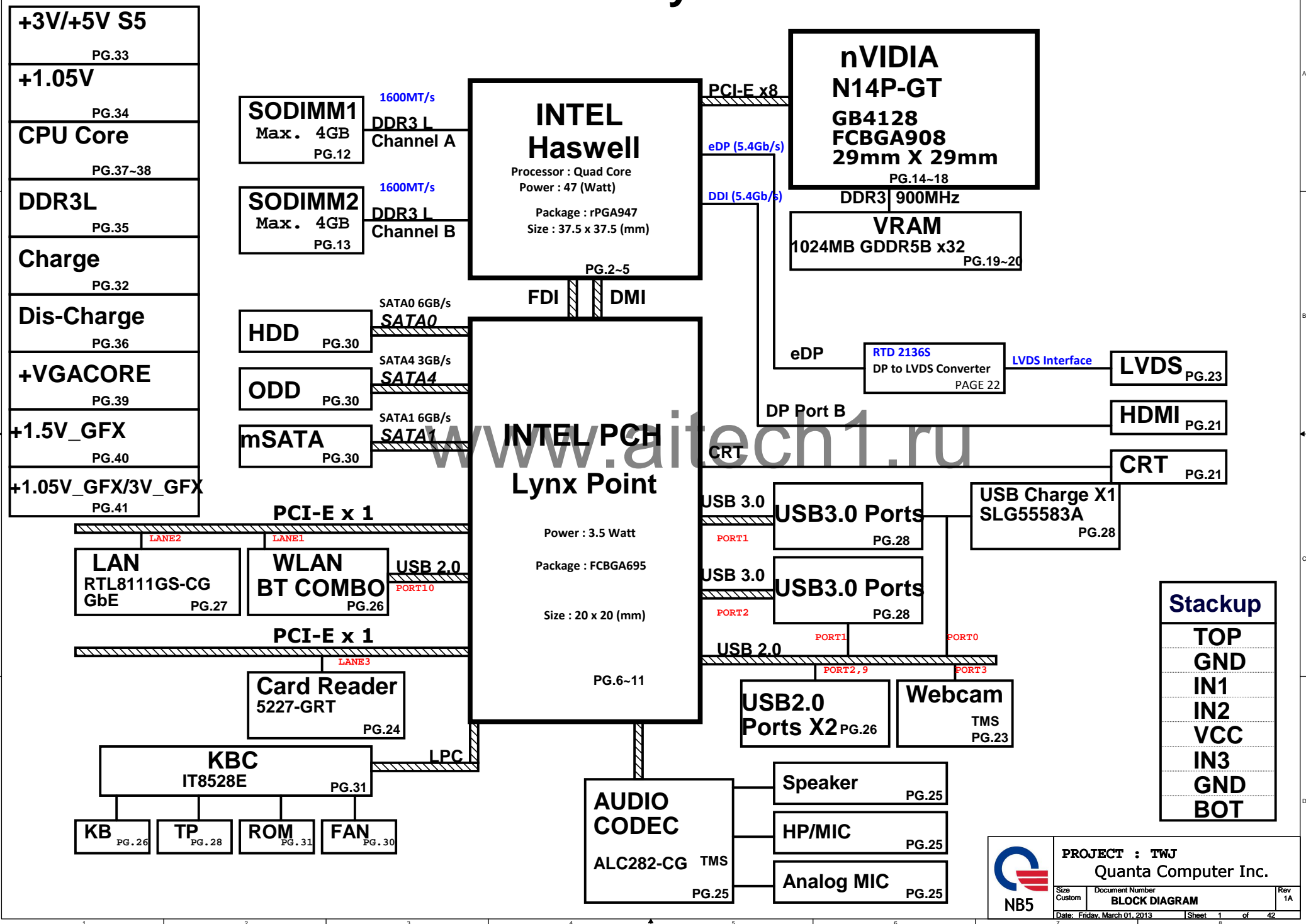
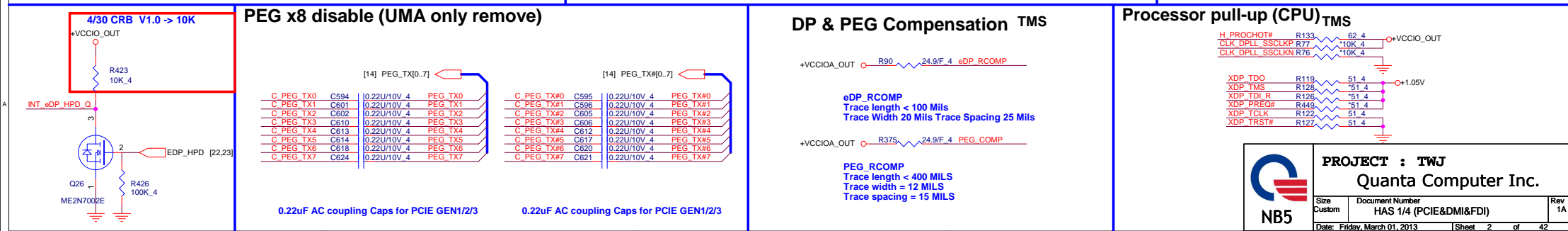
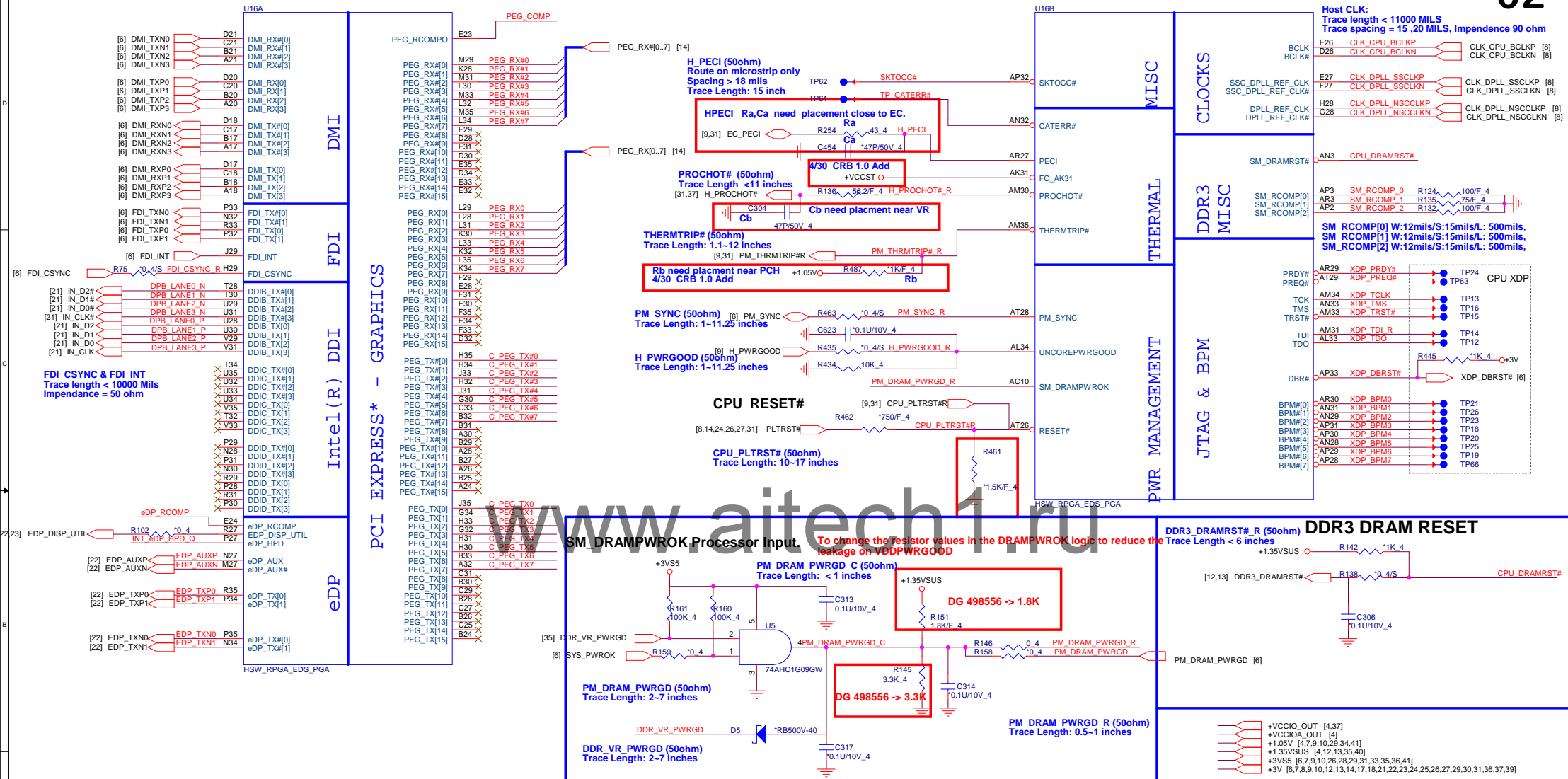


# TWJ Shark Bay DIAGRAM

01

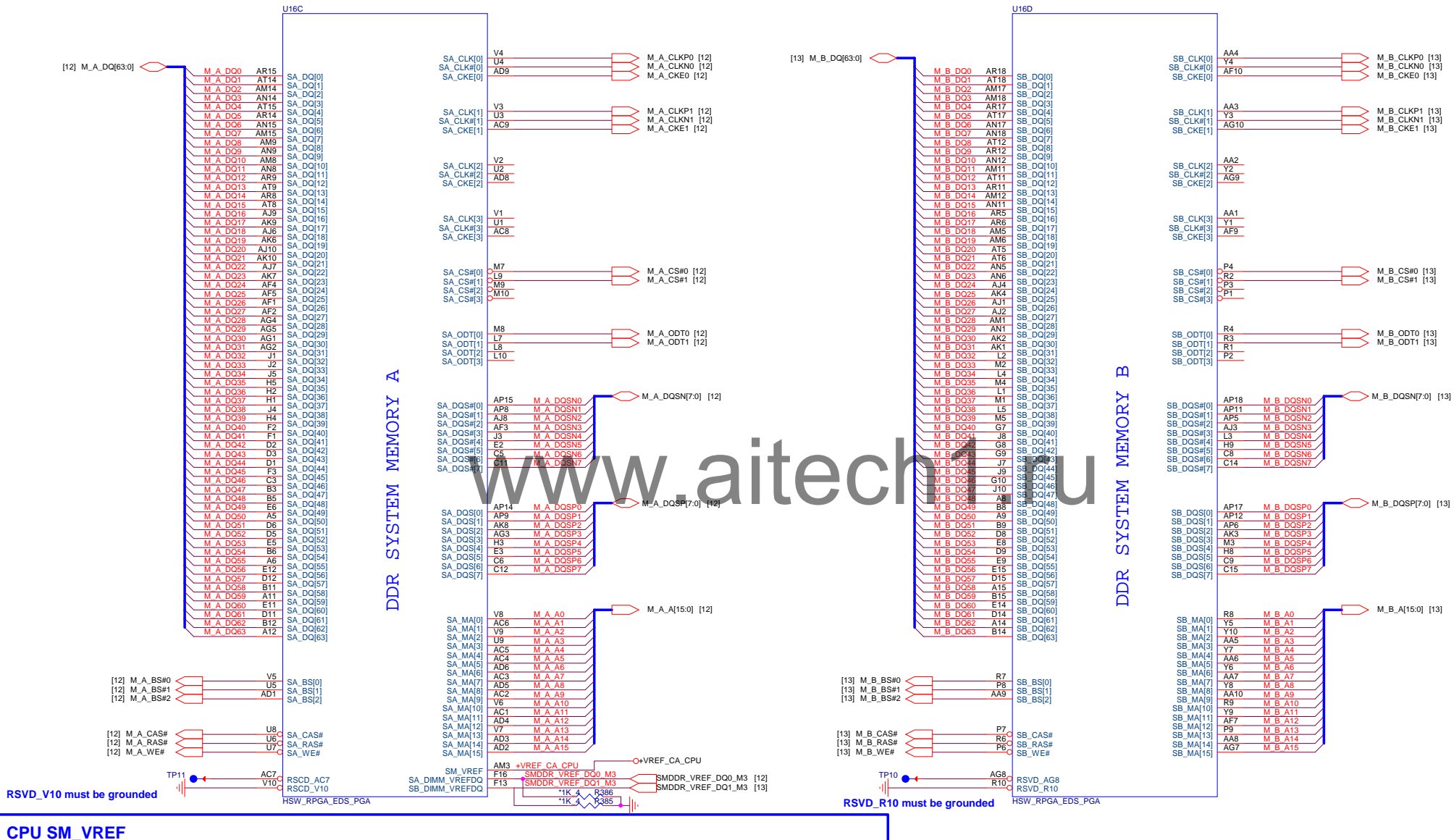




**PROJECT : TWJ**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	HAS 1/4 (PCIE&DMI&FDI)	1A
Date: Friday, March 01, 2013	Sheet 2 of 42	

## Haswell Processor (DDR3)



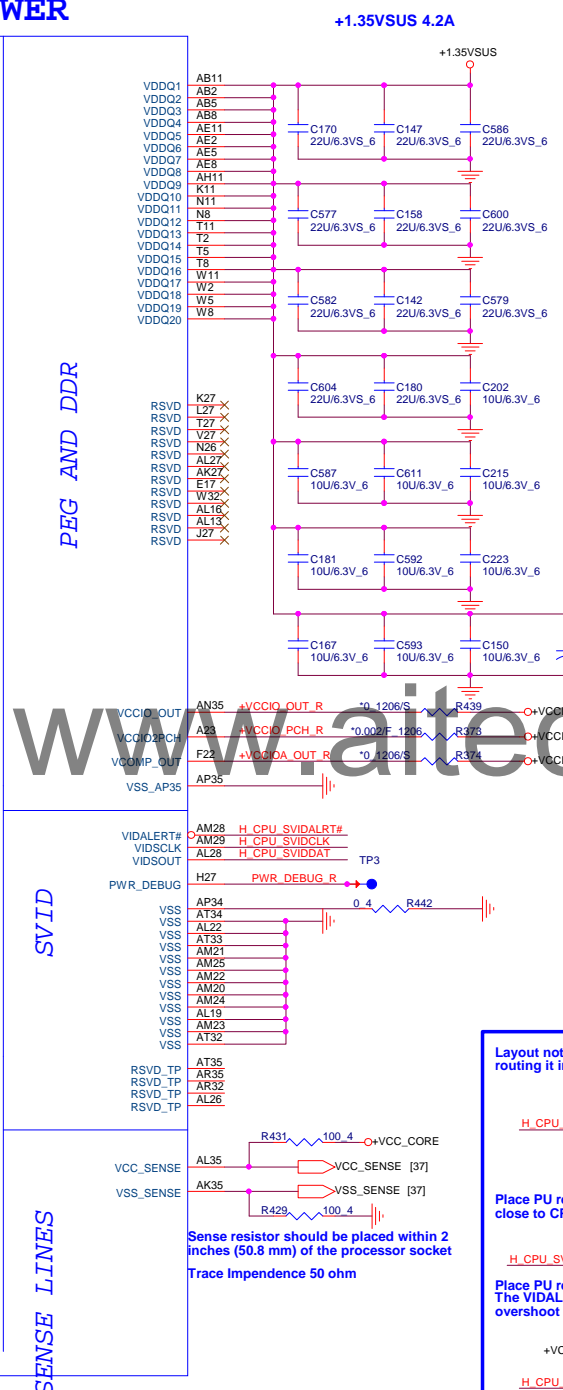
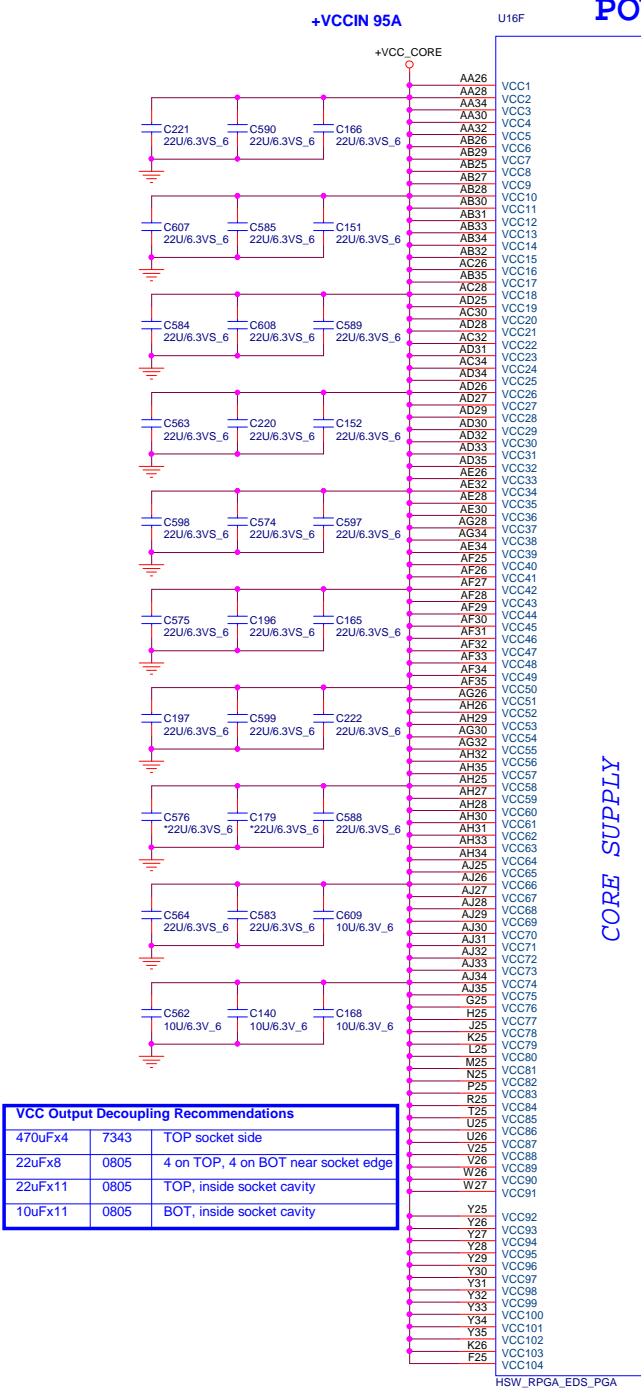
## CPU SM\_VREF

RSVD\_R10 must be grounded

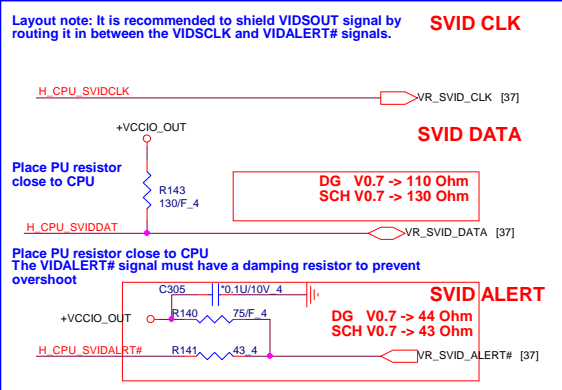
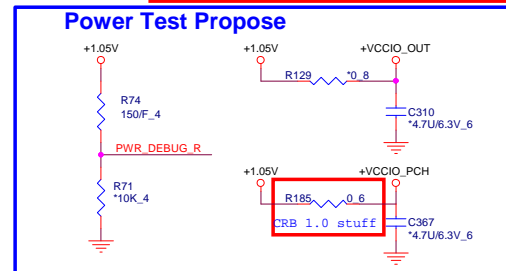
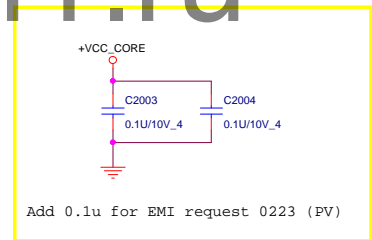
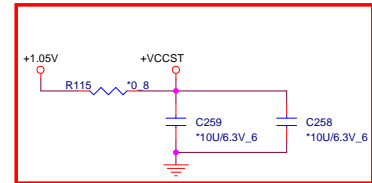
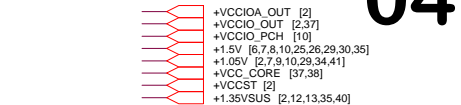
 +VREF\_CA\_CPU [12]

# Haswell Processor (POWER)

04



Capacitor	Value	Location
330uF	7343	BOT socket side
22uF	0805	5 on TOP, 6 on BOT inside socket cavity
10uF	0805	5 on TOP, 5 on BOT inside socket cavity

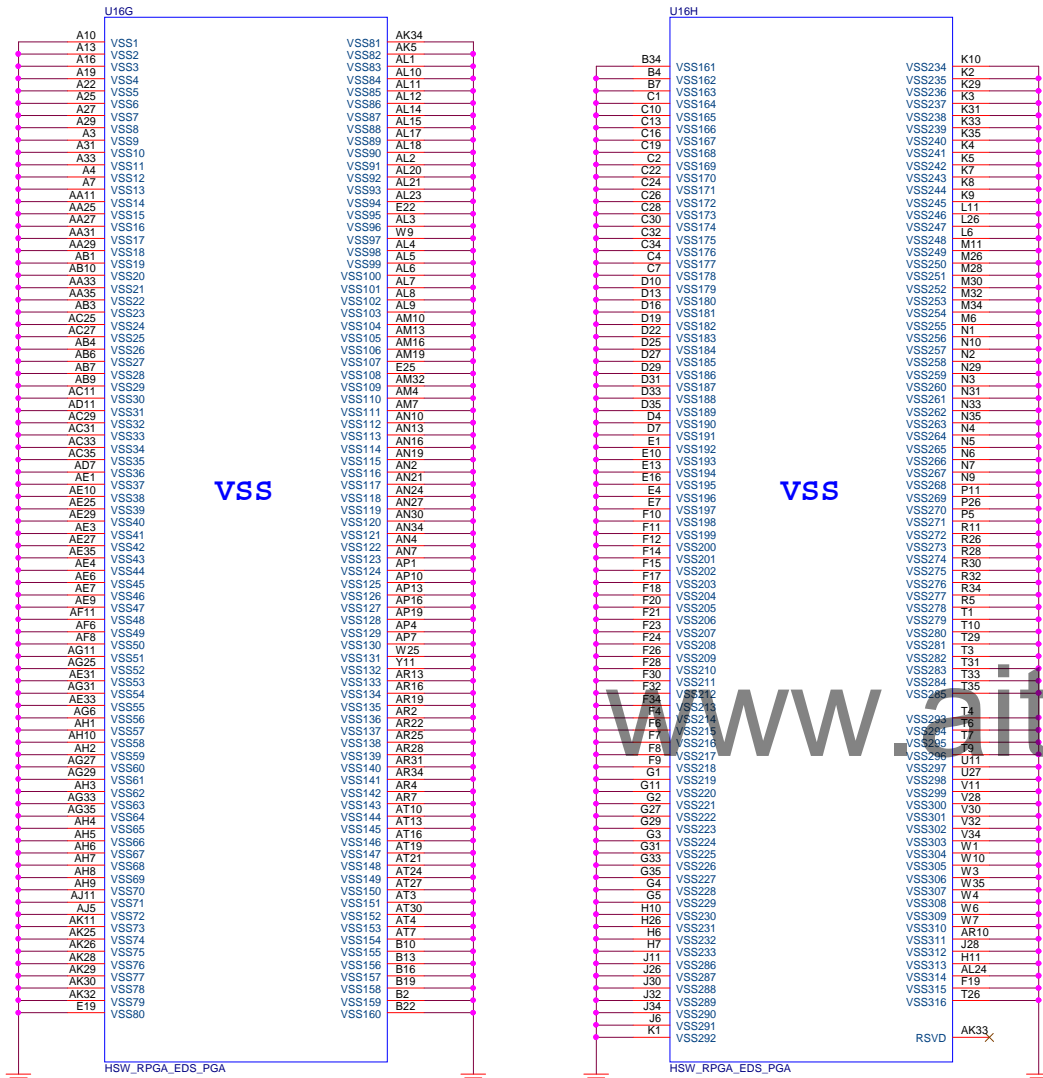


**PROJECT : TWJ**  
**Quanta Computer Inc.**

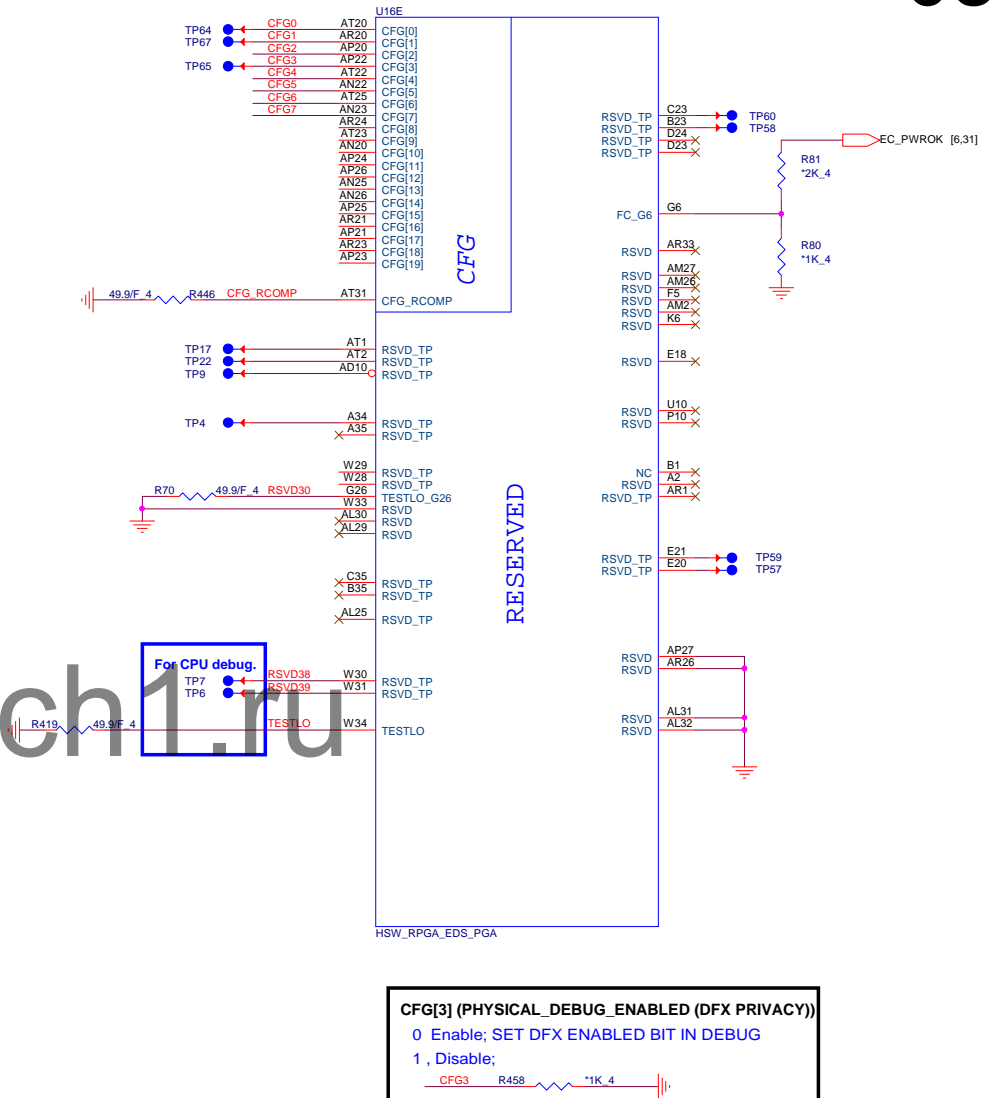
Size Custom	Document Number HAS 3/4 (POWER)	Rev 1A
Date: Friday, March 01, 2013	Sheet 4	of 42



# Haswell Processor (GND)



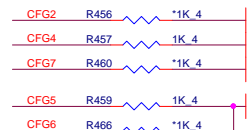
# Haswell Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

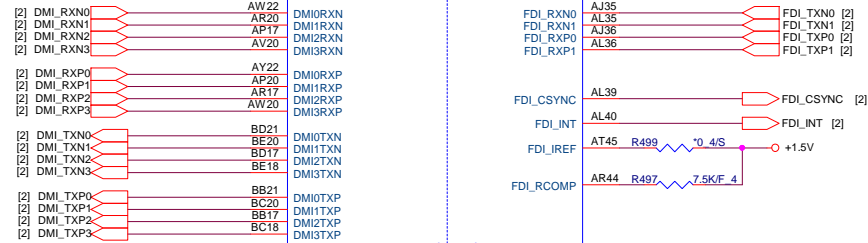


**PROJECT : TWJ**  
**Quanta Computer Inc.**

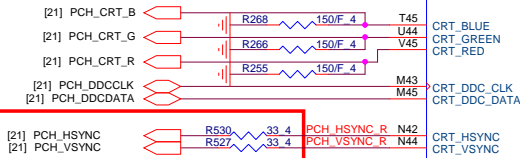
Size Custom	Document Number HAS 4/4 (GND)	Rev 1A
Date: Friday, March 01, 2013   Sheet 5 of 42		

U21C

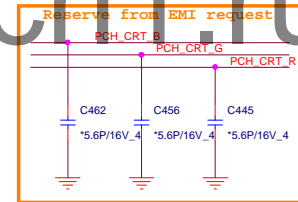
U21D



PD Res place close to PCH  
PCH to Res routing 37.5 ohm Impedance.  
Res to connector filter routing 50ohm Impedance.



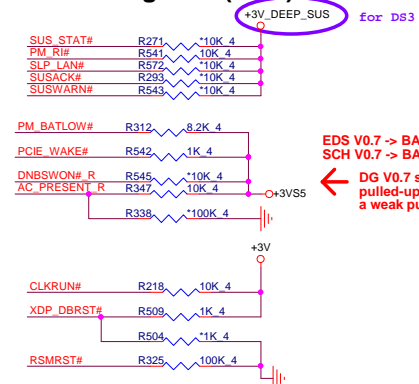
DAC\_IREF (50ohm)  
Trace length < 500 MILLS  
Trace spacing = 30 MILLS



PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

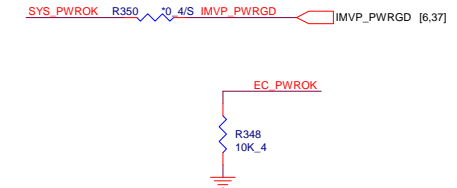
+3V\_DEEP\_SUS [7,8,9,10]  
+3V\_RTC [7,10]  
+1.5V [7,8,10,25,26,29,30,35]  
+3VS5 [2,7,9,10,26,28,29,31,33,35,36,41]  
+3V [2,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]

## PCH Pull-high/low(CLG)



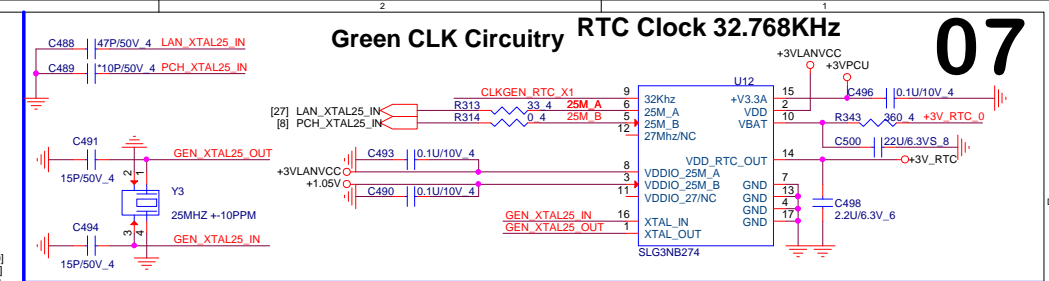
EDS V0.7 -> BATLOW# is in SUS well  
SCH V0.7 -> BATLOW# pull up to DS3 power  
DG V0.7 say that PWRBTN# is internal  
pulled-up in PCH to 3.3 V DSW through  
a weak pull-up resistor (24 kΩ nominal)

## System PWR\_OK(CLG)



On Die DSW VR Enable  
High = Enable (Default)  
Low = Disable

## 07



**ODD (SATA1 1.5Gb/s)**

**HDD0 (SATA3 6.0Gb/s)**

**mSATA (SATA3 6.0Gb/s)**

DG V0.7 -> 750 ohm  
SCH V0.7 -> 0 ohm

BD4 SATA\_IREF R217 0 4

EM:

## HDA Bus(CLG)

## PCH JTAG Debug(CLG)

3V55

R522 '210F\_4

R520 '210F\_4

R524 '210F\_4

R523 '100F\_4

R519 '100F\_4

R525 '100F\_4

R529 '51\_4

PCH JTAG TMS

PCH JTAG TDI R

PCH JTAG TDO R


PCH JTAG TCK R

## PCH SPI ROM(CLG)

### PCH SPI ROM(CLG)

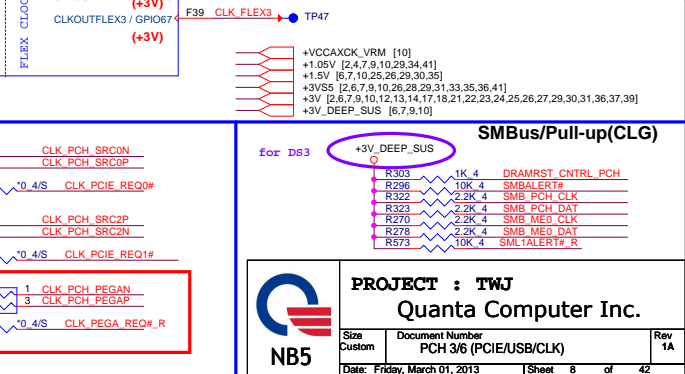
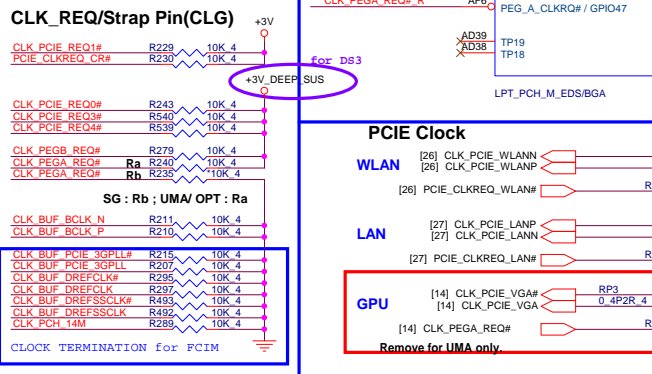
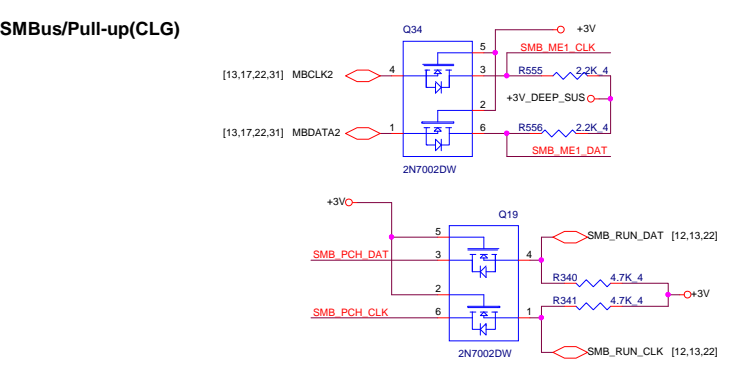
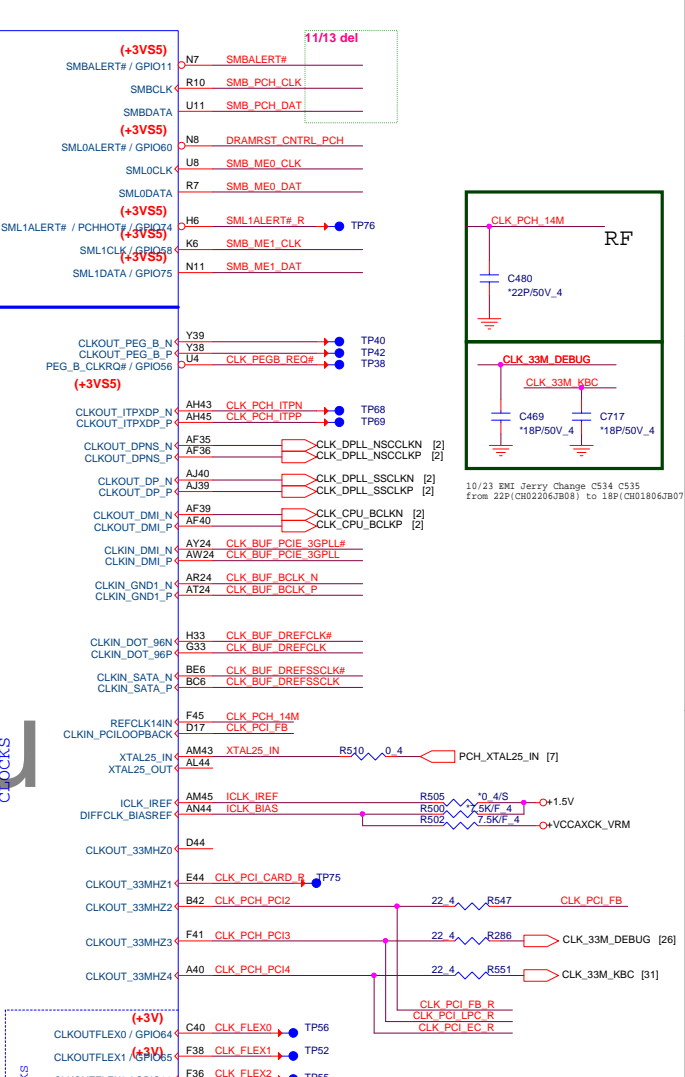
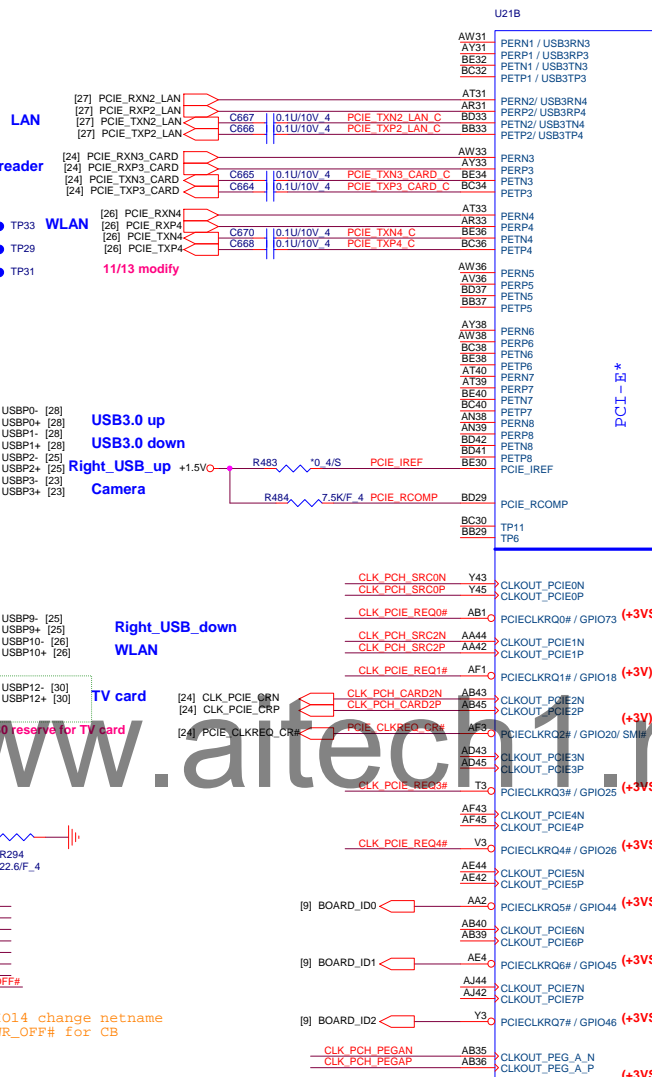
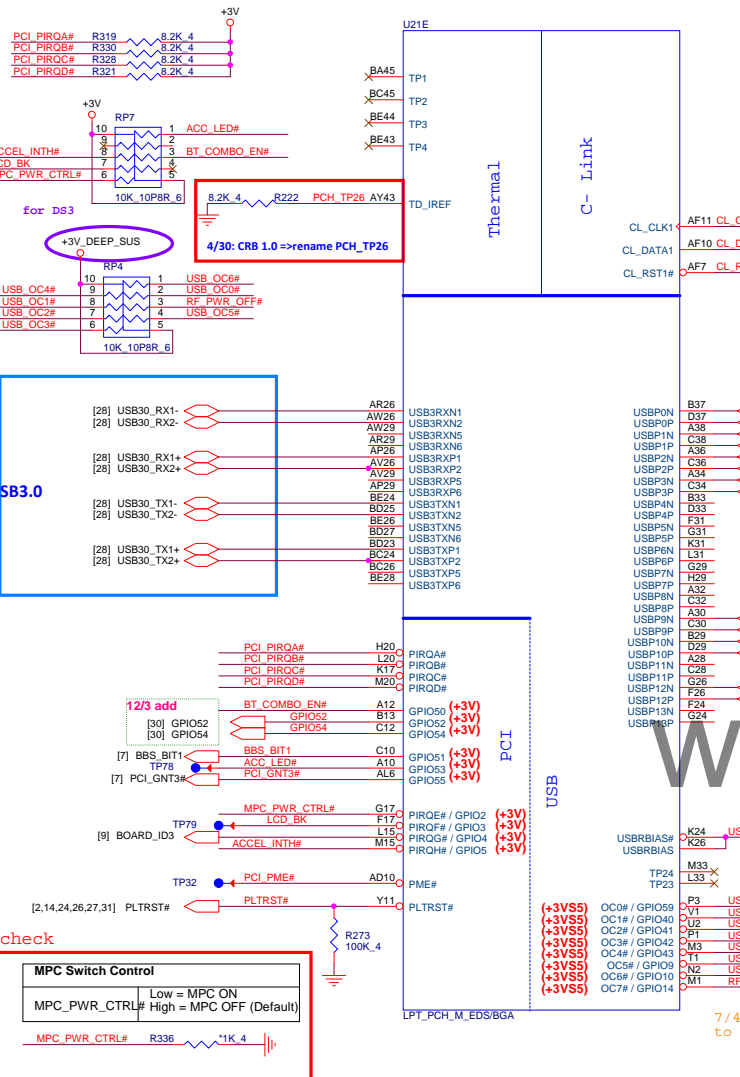
The schematic diagram illustrates the PCH SPI ROM (CLG) circuit. It features a U10 (A25LQ16M-FQ) component connected to various signals and power sources. The connections are as follows:

- U10 (A25LQ16M-FQ) Pins:**
  - Pin 1 (CE#) is connected to PCH\_SPI\_CS0# via R272 (0.4).
  - Pin 2 (SCK) is connected to PCH\_SPI\_CLK via R288 (0.4).
  - Pin 3 (SI) is connected to PCH\_SPI\_SI via R291 (0.4).
  - Pin 4 (SO) is connected to PCH\_SPI\_SO via R282 (0.4).
  - Pin 5 (WP#) is connected to PCH\_SPI\_CS0# via R289 (0.4).
  - Pin 6 (VDD) is connected to +3V.
  - Pin 7 (HOLD#) is connected to +3V.
  - Pin 8 (VSS) is connected to ground.
- Other Components:**
  - TP39, TP35, TP44, TP51 are test points connected to the SPI lines.
  - C475 and C478 are 22pF capacitors connected to ground.
  - C466 is a 0.1uF capacitor connected to ground.
  - TP43 is a test point connected to the SPI lines.
  - TP41 is a test point connected to the SPI lines.
  - R237, R234, R287, and R283 are resistors (0.4, 0.4, 1K, 1K) connected to the SPI lines.

 <b>NB5</b>	<b>PROJECT : TWJ</b> <b>Quanta Computer Inc.</b>		
	Size	Document Number	Rev
	Custom	PCH 2/6 (SATA/HDA/SPI)	1A
	Date: Friday, March 01, 2013	Sheet 7 of 42	

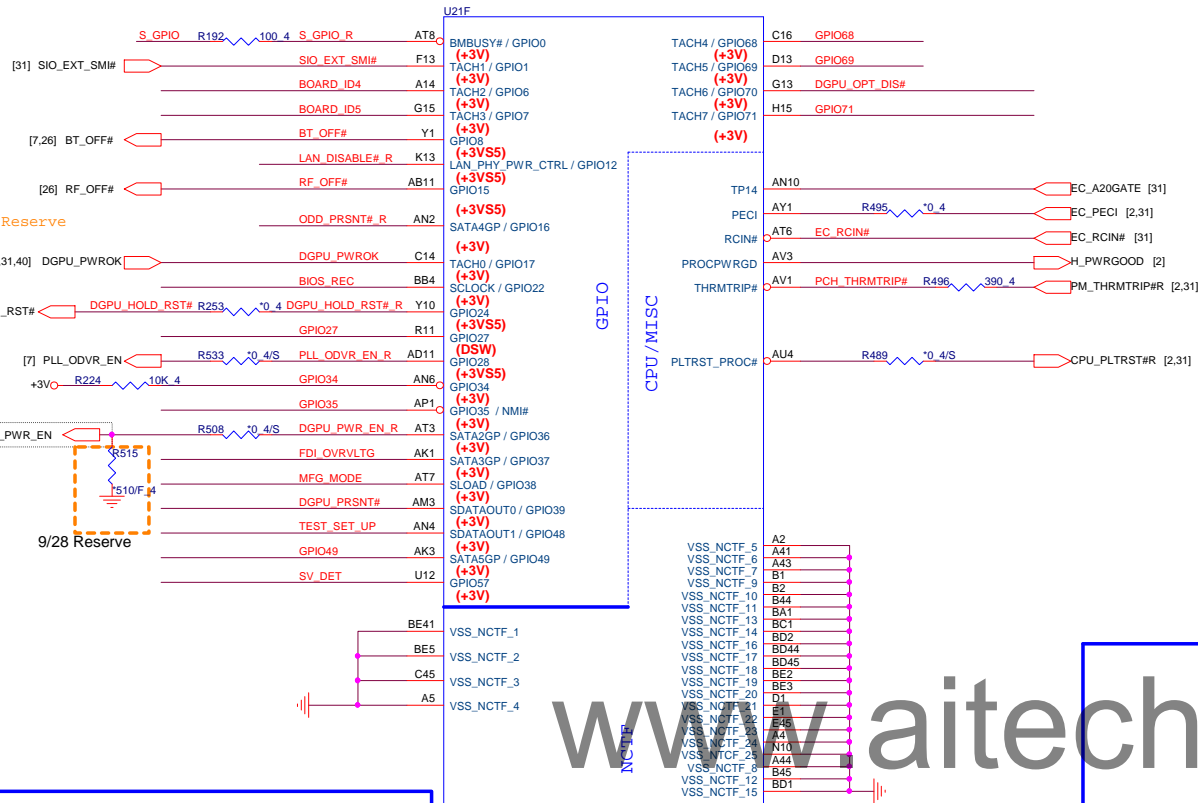


NB5



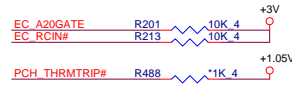
# Lynx Point (GPIO,VSS\_NCTF,RSVD)

09

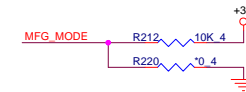


+3V DEEP\_SUS [6,7,8,10]  
+3VSS [2,6,7,10,26,28,29,31,33,35,36,41]  
+3V [2,6,7,8,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]  
+5VSS [25,28,29,33,34,35,36,37,38,39,40]

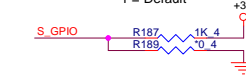
## PCH MISC PU/PD



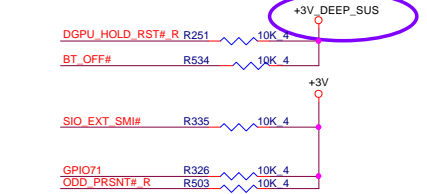
## MFG-TEST



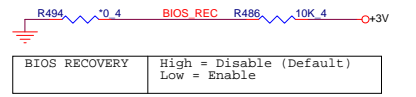
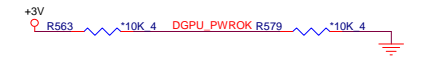
## Swap GPIO



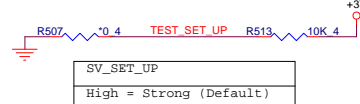
## GPIO Pull-up/Pull-down(CLG)



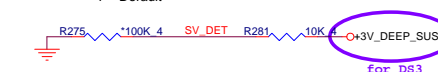
## DGPU\_PWROK UMA=0



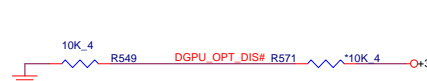
## BIOS\_RESP



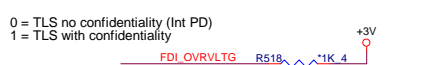
## SV Detect



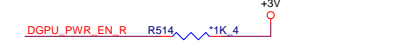
## DGPU\_OPT\_DIS# GPIO70 Optimus=0, Dis only=1



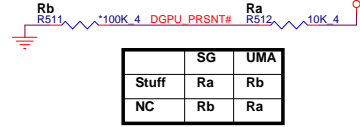
## SATA3GP/GPIO37 TLS Confidentiality



## GPIO36 Internal PD



## GFX Present GPIO39 Optimus=1, UMA=0



## HSW BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO4	MODEL BIT3
BOARD_ID4	GPIO6	MODEL BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRST	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

BOARD_ID[4:0]	Model Name
00000	QLGS
00001	TWS
00010	TWJ
GPIO68	Hi
GPIO68	Lo
GPIO68	LVDS interface
GPIO68	eDP interface

**PROJECT : TWJ**  
**Quanta Computer Inc.**

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Friday, March 01, 2013	Sheet 9 of 42	



# Lynx Point (POWER)

## POWER

### USB

### GPIO/LPC

### Thermal

### CPU

### RTC

### SATA

### HDA

### FUSE

### USB3

### FDI

### SPI

### USB3

### FDI

### SPI

### USB3

### FDI

### SPI

### USB3

### FDI

### SPI

### USB3

### FDI

### SPI

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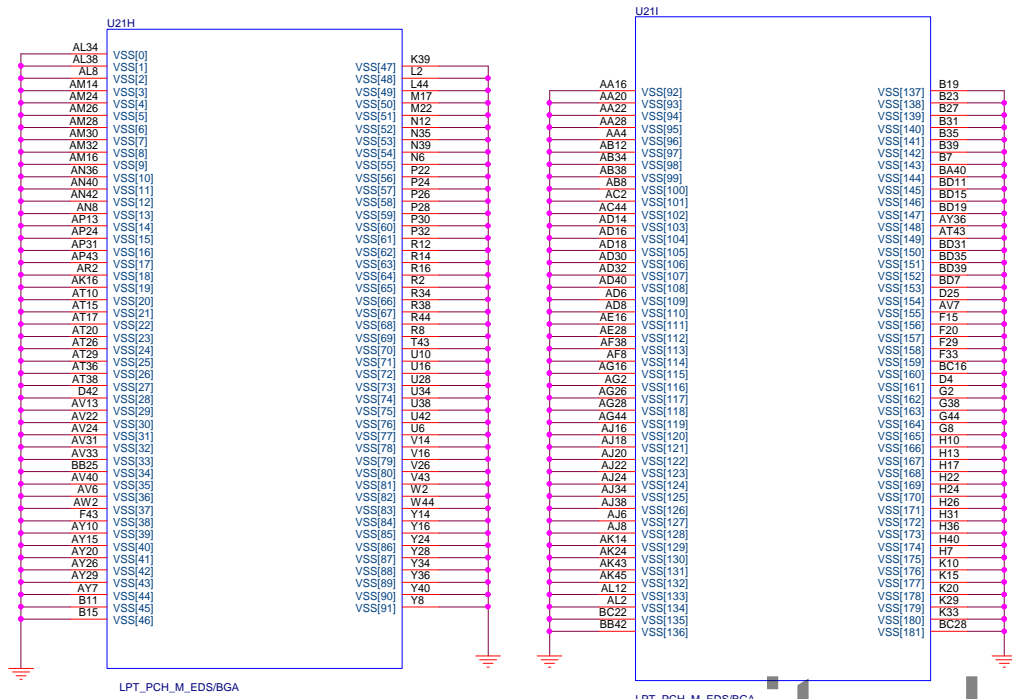
### SPI

### USB3

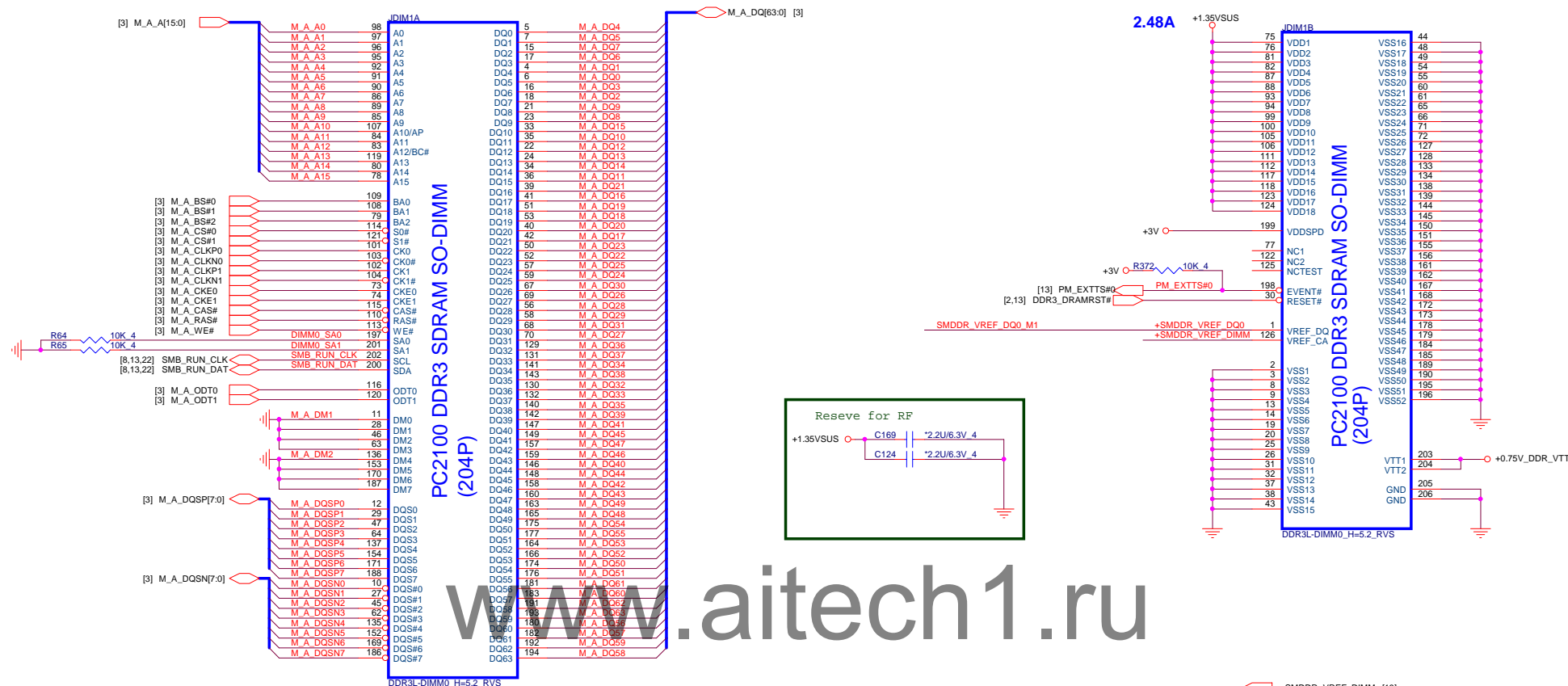
### FDI

# Lynx Point (GND)

11

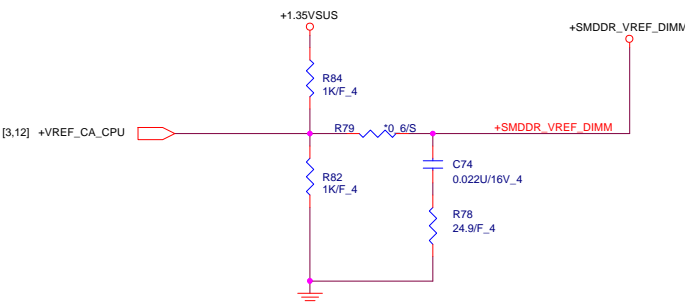


www.aitech1.ru

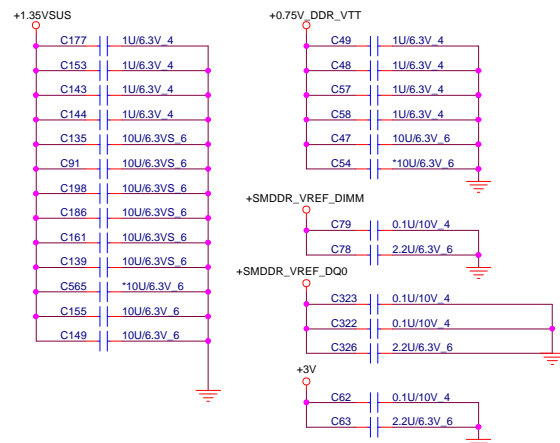


+VREF\_CA\_CPU [3,12]

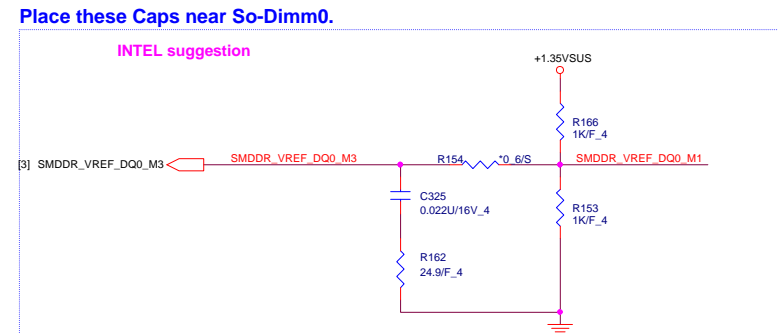
10/4 : INTEL suggestion



Place these Caps near So-Dimm0.

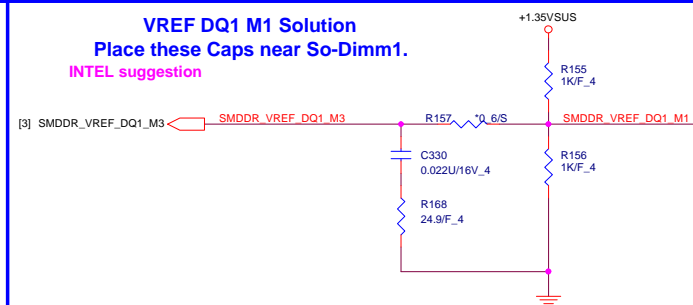
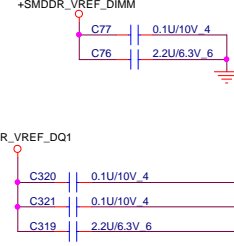
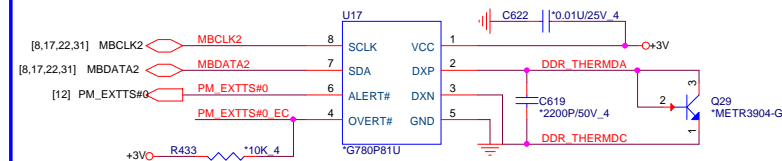


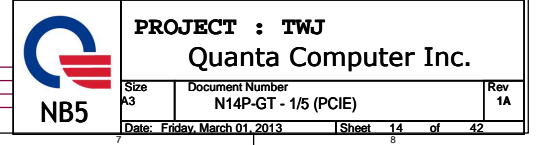
VREF DQ0 M1 Solution



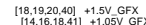
**PROJECT : TWJ**  
**Quanta Computer Inc.**

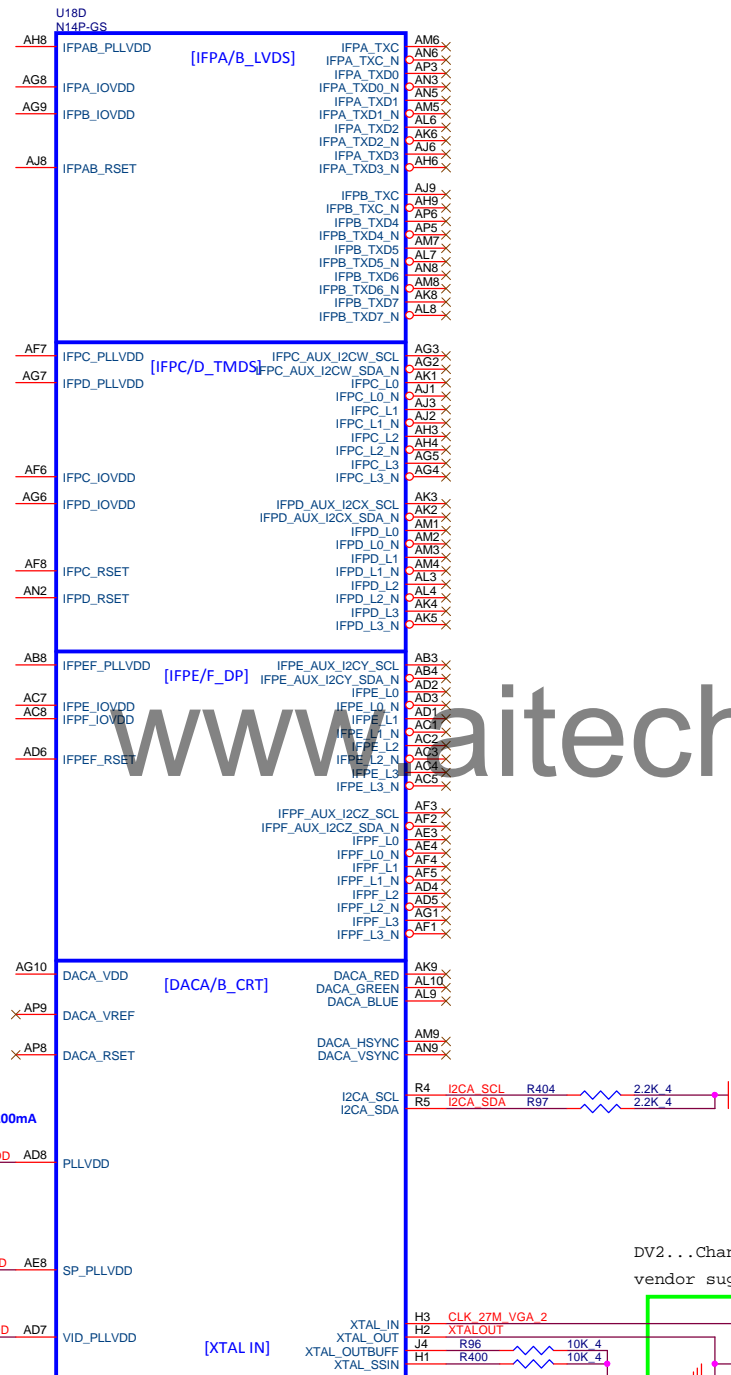
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A
Date: Friday, March 01, 2013	Sheet 12 of 42	











**PROJECT : TWJ**  
**Quanta Computer Inc.**

Size A3	Document Number N14P-GT - 3/5 (Display)	Rev 1A
Date: Friday, March 01, 2013	Sheet 16 of 42	

U18E  
N14P-GS

[MIOA]

[MIOB]

[MISC\_GPIO/I2C/JTAG/THER]

[MISC2\_ROM]

MULTISTRAP\_REF\_GND

Default: GDDR5 Hynix 2G VRAM

Vendor	P/N	Mfr. P/N	ROM_SI	
Hynix (1.5V)	AKG5MWUTW10	H5GQ2H24AFR-T2C	0100	24.9K PD
Hynix (1.35V)	AKG5MWUTW10	H5GQ2H24AFR-T2C	0110	34.8K PD
Samsung (1.5V)	AKG5MWDT505	K4G20325FD-FC04	0101	30.1K PD
Samsung (1.35V)	AKG5MWDT505	K4G20325FD-FC04	0111	45.3K PD

N14P-GT QS device ID=0x0FE4

Netname	N14P-GT
ROM_SO	4.99K PU
ROM_SCLK	15K PD
STRAP0	45.3K PU
STRAP1	4.99K PD
STRAP2	24.9K PD
STRAP3	4.99K PD
STRAP4	45.3K PD

4.99K/F\_4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)  
 10K/F\_4: CS31902FB26 RES CHIP 10K 1/16W +1% (0402)  
 15K/F\_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)  
 20K/F\_4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)  
 24.9K/F\_4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)  
 30.1K/F\_4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)  
 34.8K/F\_4: CS33482B22 RES CHIP 34.8K 1/16W +1% (0402)  
 45.3K/F\_4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

## Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMBLALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	SGIO_PADCFG[3]	SGIO_PADCFG[2]	SGIO_PADCFG[1]	SGIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHAN GE_GEN3	PCI_MAX_SPEED	DP_PLL_VDD33V

Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDQ2	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V / 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V / 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V / 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V / 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

## GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

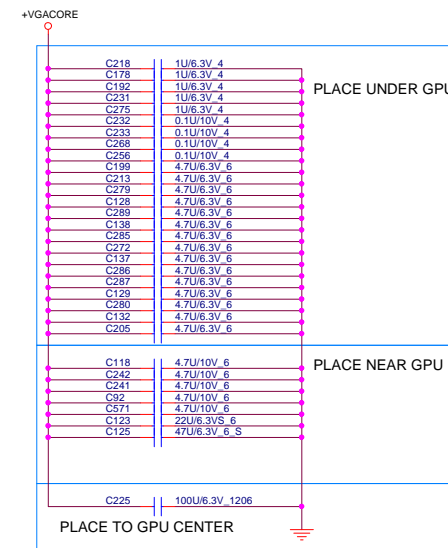
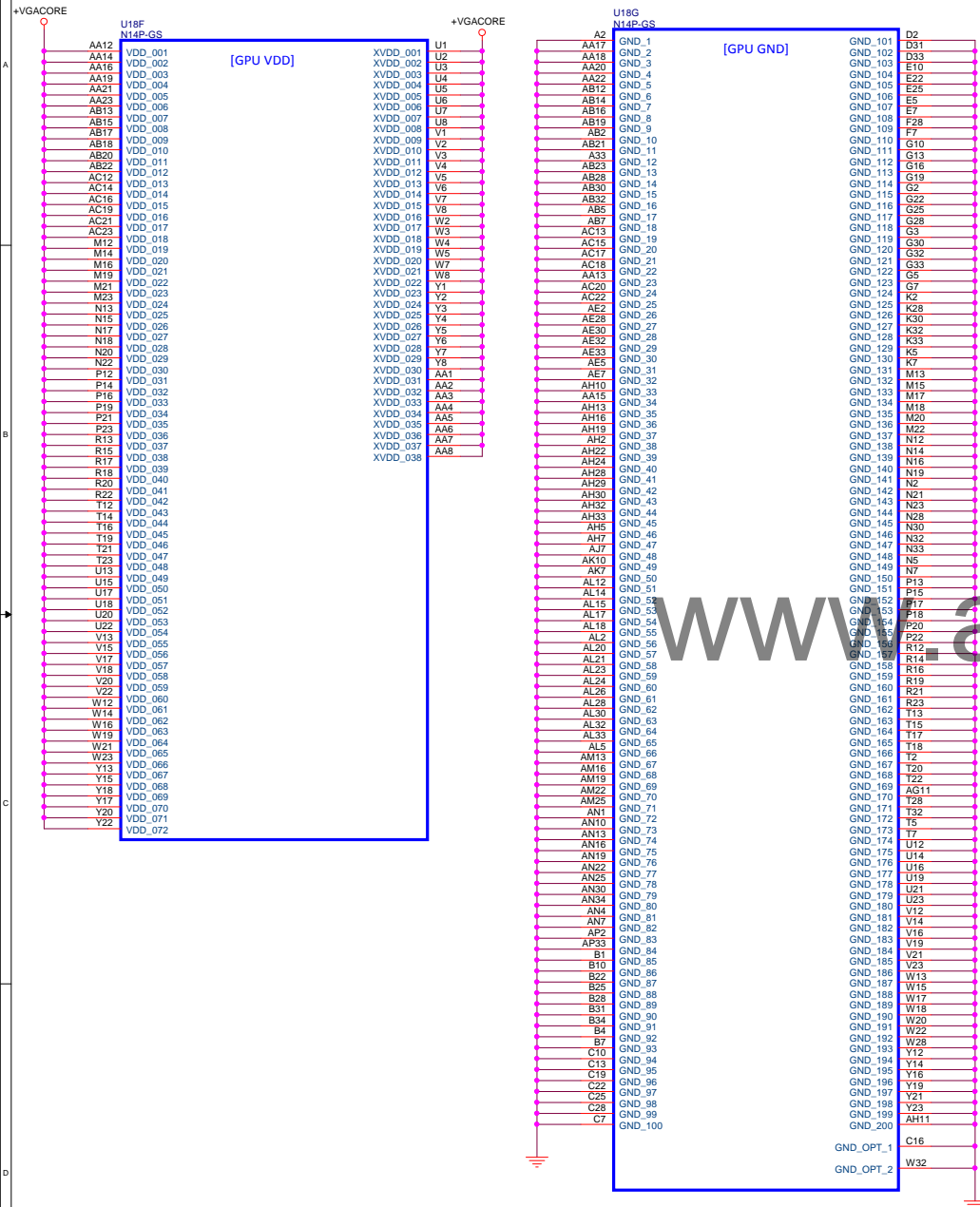


**PROJECT : TWJ**  
**Quanta Computer Inc.**

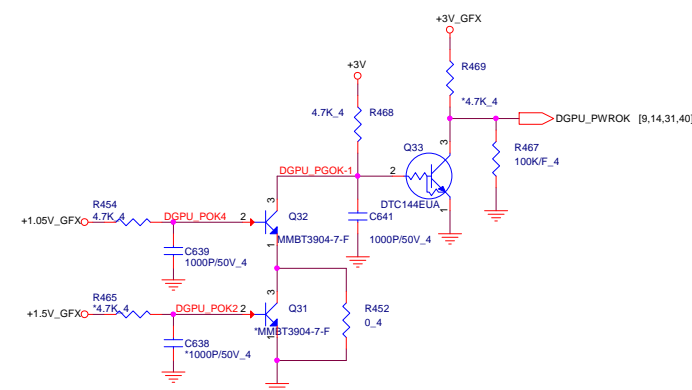
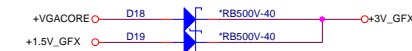
Size Custom	Document Number	Rev
	N14P-GT - 4/5 (MISC)	1A
Date: Friday, March 01, 2013	Sheet 17 of 42	

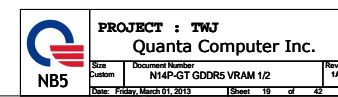
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VDD/XVDD : 25.72A



for meet Power down sequence for +3V\_GFX







Channel 0  
<0-31>Channel 0  
<32-63>Channel 1  
<0-31>

MF=1 Mirrored

MF=0 Non-mirrored

MF=1 Mirrored

MF=0 Non-mirrored

[15] VMC\_DQ63[0..] VMC\_DQ63[0..]  
[15] FBC\_CMD3[10..] FBC\_CMD3[10..]  
[15] FBC\_CMD7[0..] FBC\_CMD7[0..]  
[15] FBC\_EDC7[0..] FBC\_EDC7[0..]

QD16~23

QD8~15

QD48~55

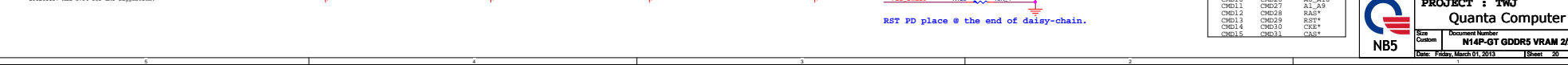
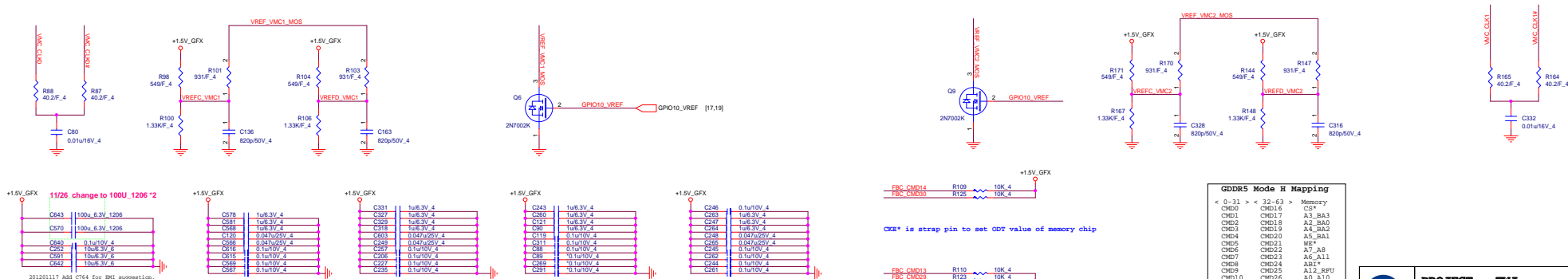
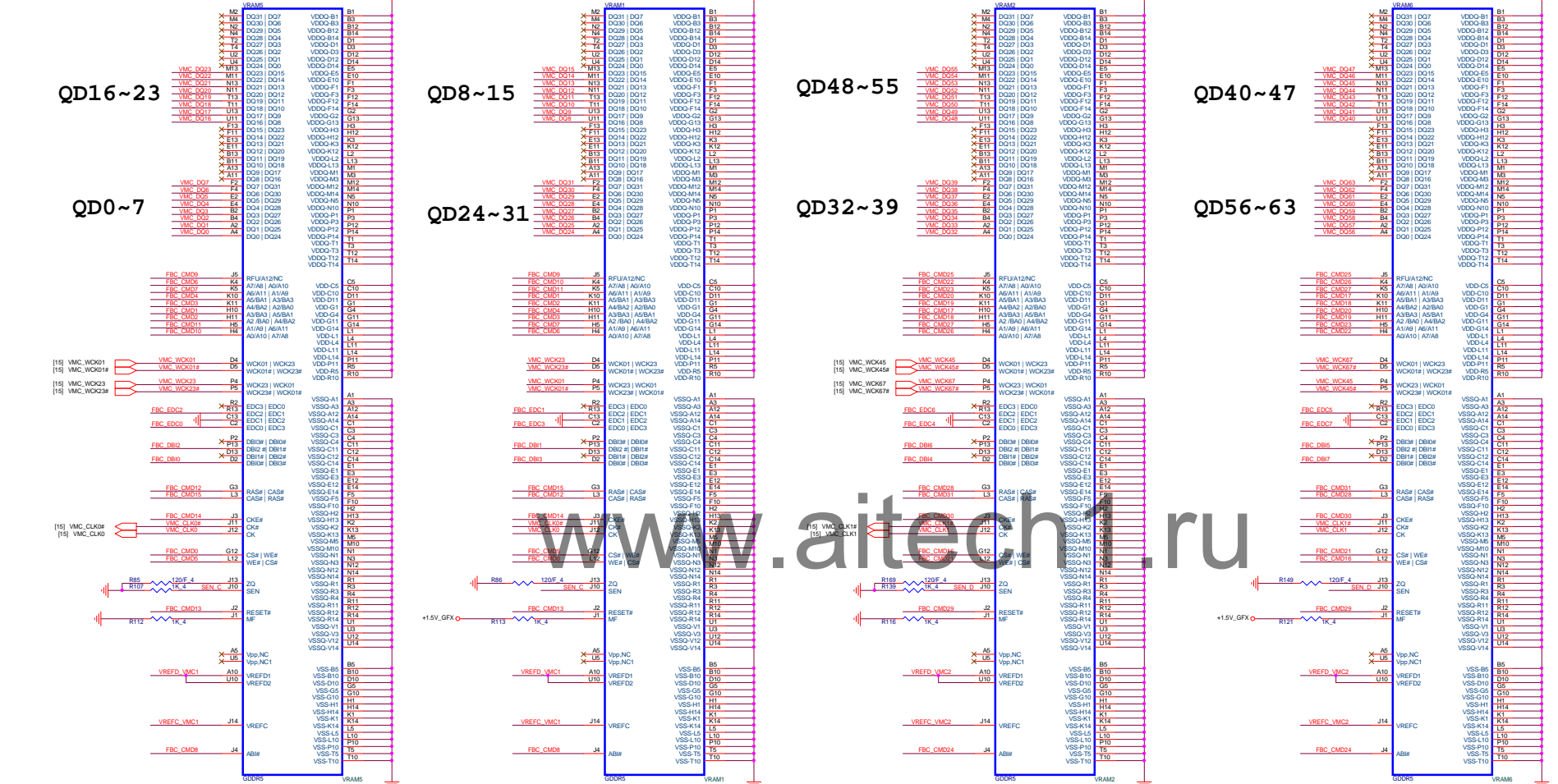
QD40~47

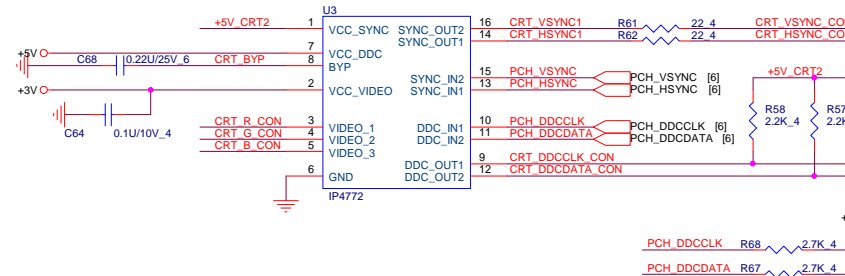
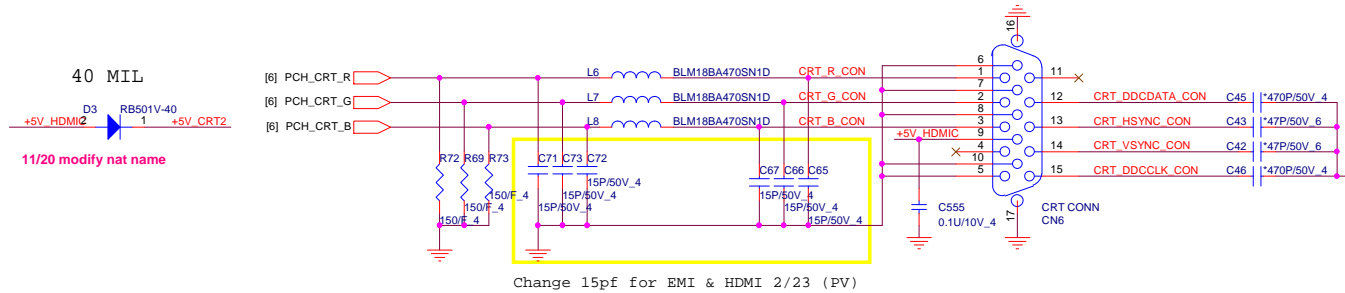
QD0~7

QD24~31

QD32~39

QD56~63

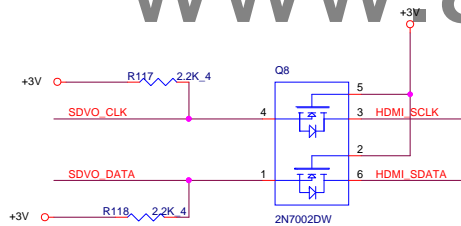




## HDMI PORT

close to HDMI conn

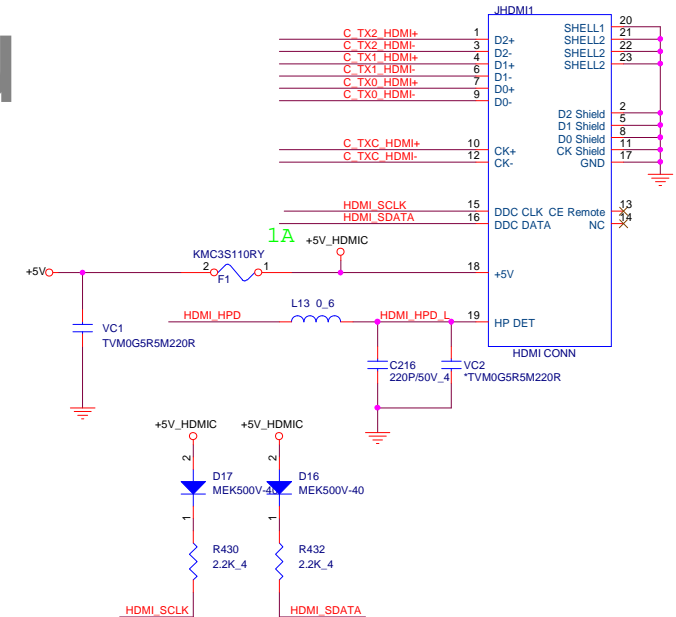
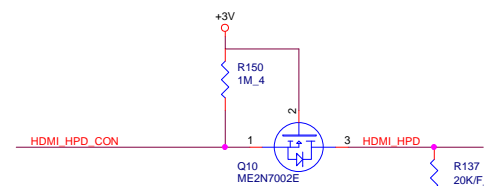
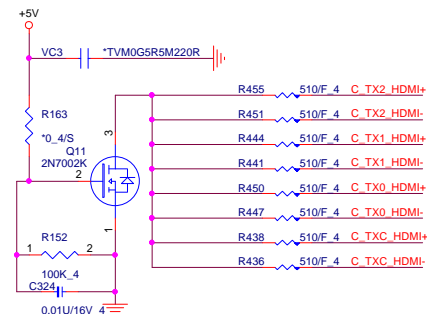
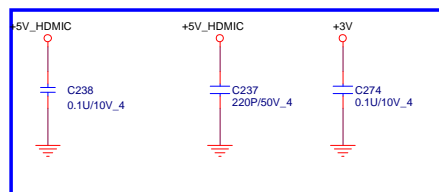
[2] IN_CLK#	IN_CLK#	C625	0.1U/10V_4	C TXC HDMI-
[2] IN_CLK	IN_CLK	C626	0.1U/10V_4	C TXC HDMI+
[2] IN_D0#	IN_D0#	C631	0.1U/10V_4	C TX0 HDMI-
[2] IN_D0	IN_D0	C632	0.1U/10V_4	C TX0 HDMI+
[2] IN_D1#	IN_D1#	C627	0.1U/10V_4	C TX1 HDMI-
[2] IN_D1	IN_D1	C628	0.1U/10V_4	C TX1 HDMI+
[2] IN_D2#	IN_D2#	C635	0.1U/10V_4	C TX2 HDMI-
[2] IN_D2	IN_D2	C637	0.1U/10V_4	C TX2 HDMI+



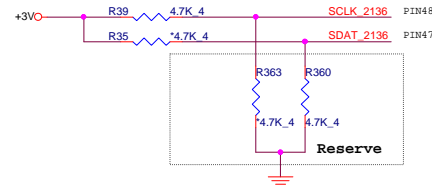
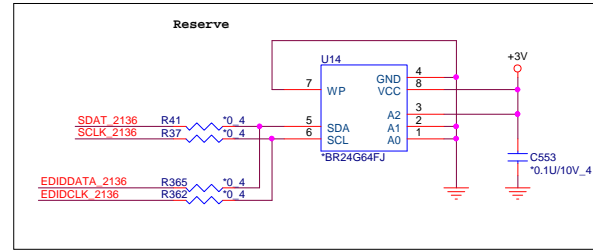
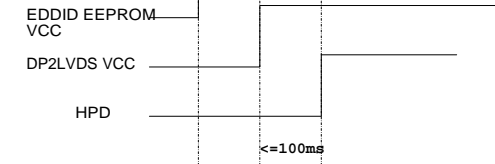
EMI request			
C TX2 HDMI+	R453	150/F_4	C TX2 HDMI-
C TX1 HDMI+	R443	150/F_4	C TX1 HDMI-
C TX0 HDMI+	R448	150/F_4	C TX0 HDMI-
C TXC HDMI+	R437	150/F_4	C TXC HDMI-

[6] SDVO_CLK	SDVO_CLK	SDVO_DATA
[6] SDVO_DATA	SDVO_DATA	HDMI_HPDCON

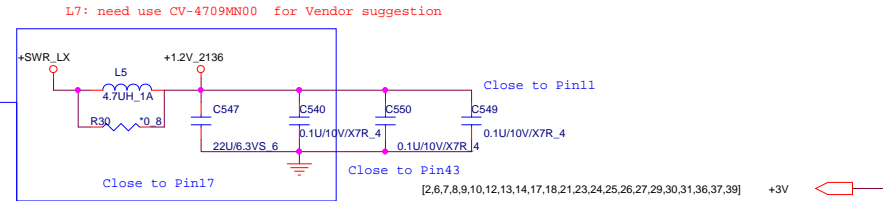
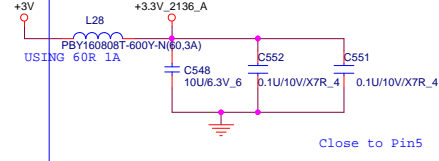
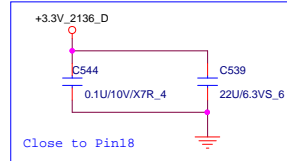
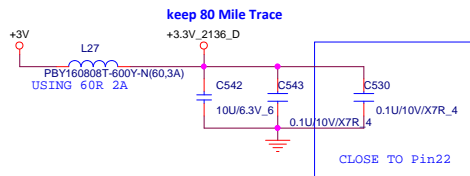
## EMI request



PROJECT : TWJ	
Quanta Computer Inc.	
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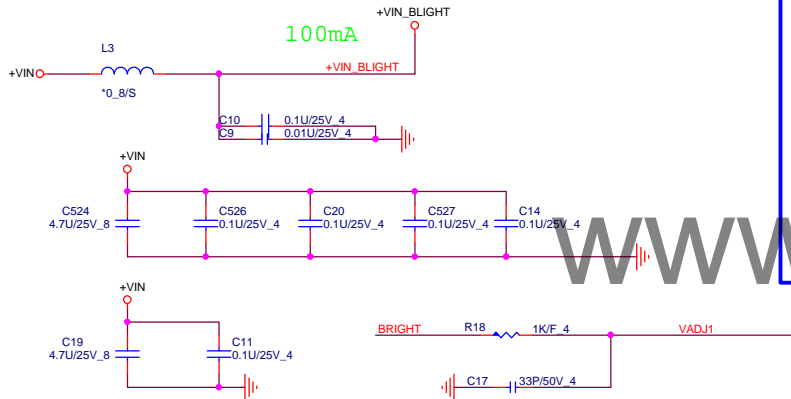
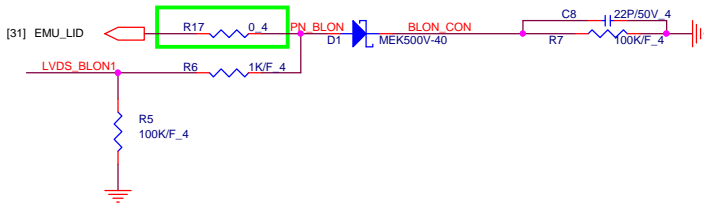
		PIN 47	
		0	1
PIN 48	0	X	EP mode
	1	ROM	EEPROM



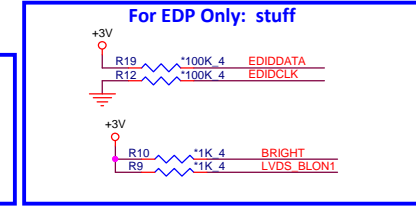
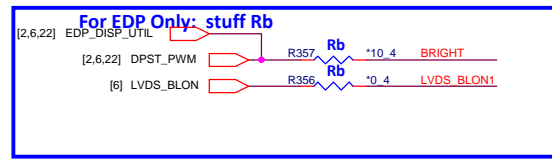
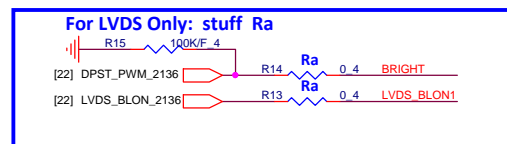
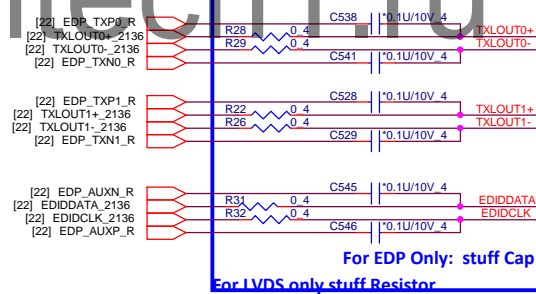
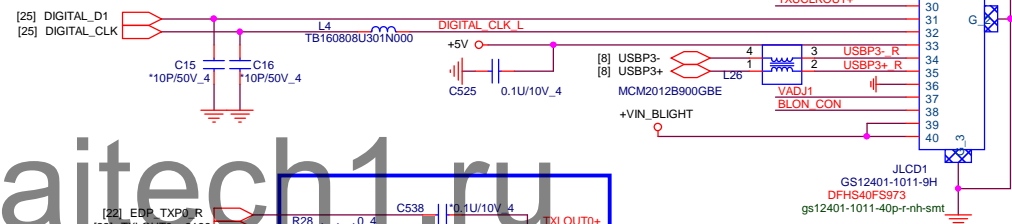
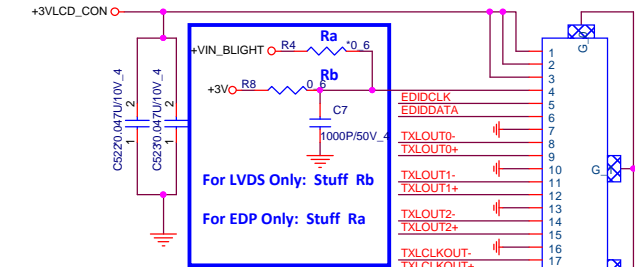
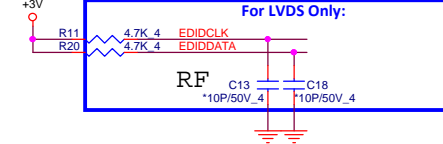
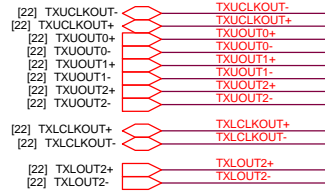
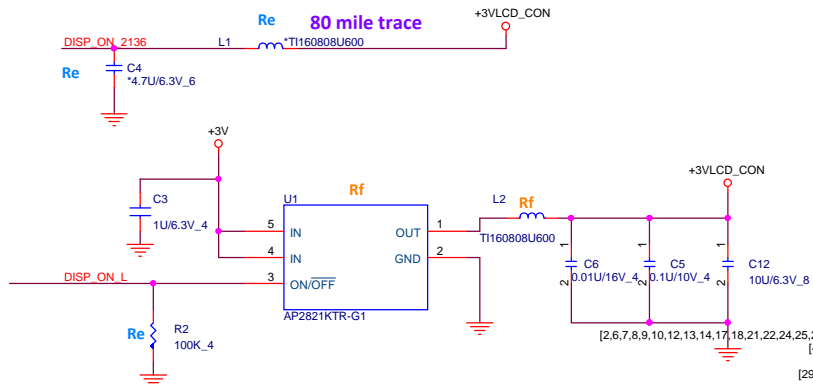
SWR MODE	LDO MODE
Stuff L69	Stuff R9095

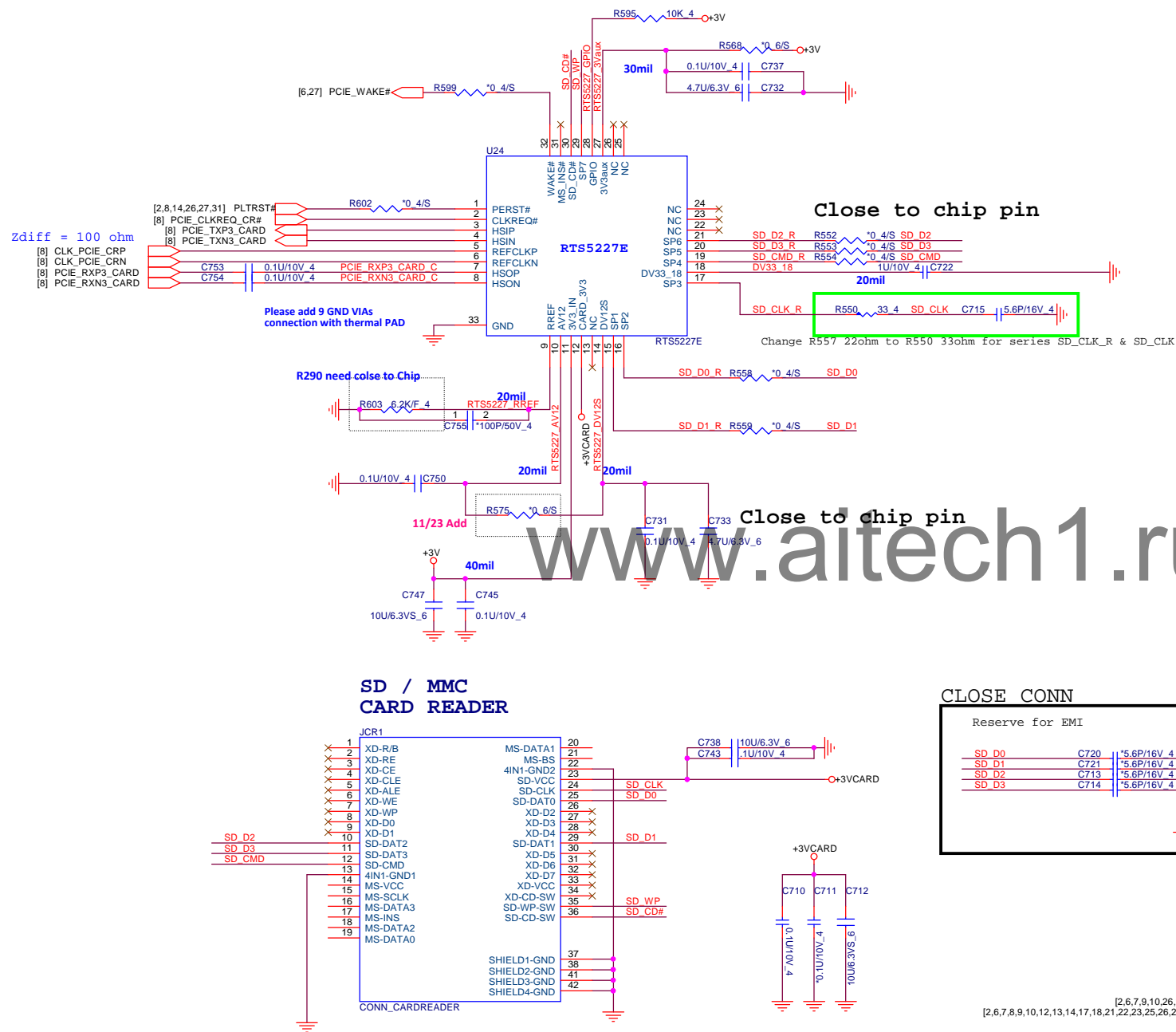
# LID Switch

23

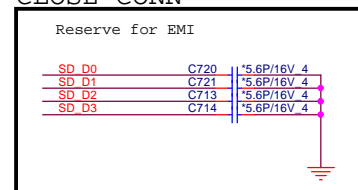


[6] DISP\_ON R1 Rd \*0.4 DISP\_ON L  
 [22] DISP\_ON\_2136 R3 Rc 0.4 DISP\_ON L  
 For EDP Only: stuff Rd,Rf  
 For LVDS Only use power switch: stuff Rc,Rf  
 For LVDS Only non-use power switch: stuff Re





CLOSE CONN



[2,6,7,9,10,26,28,29,31,33,35,36,41] +3VS5  
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,25,26,27,29,30,31,36,37,39] +3V

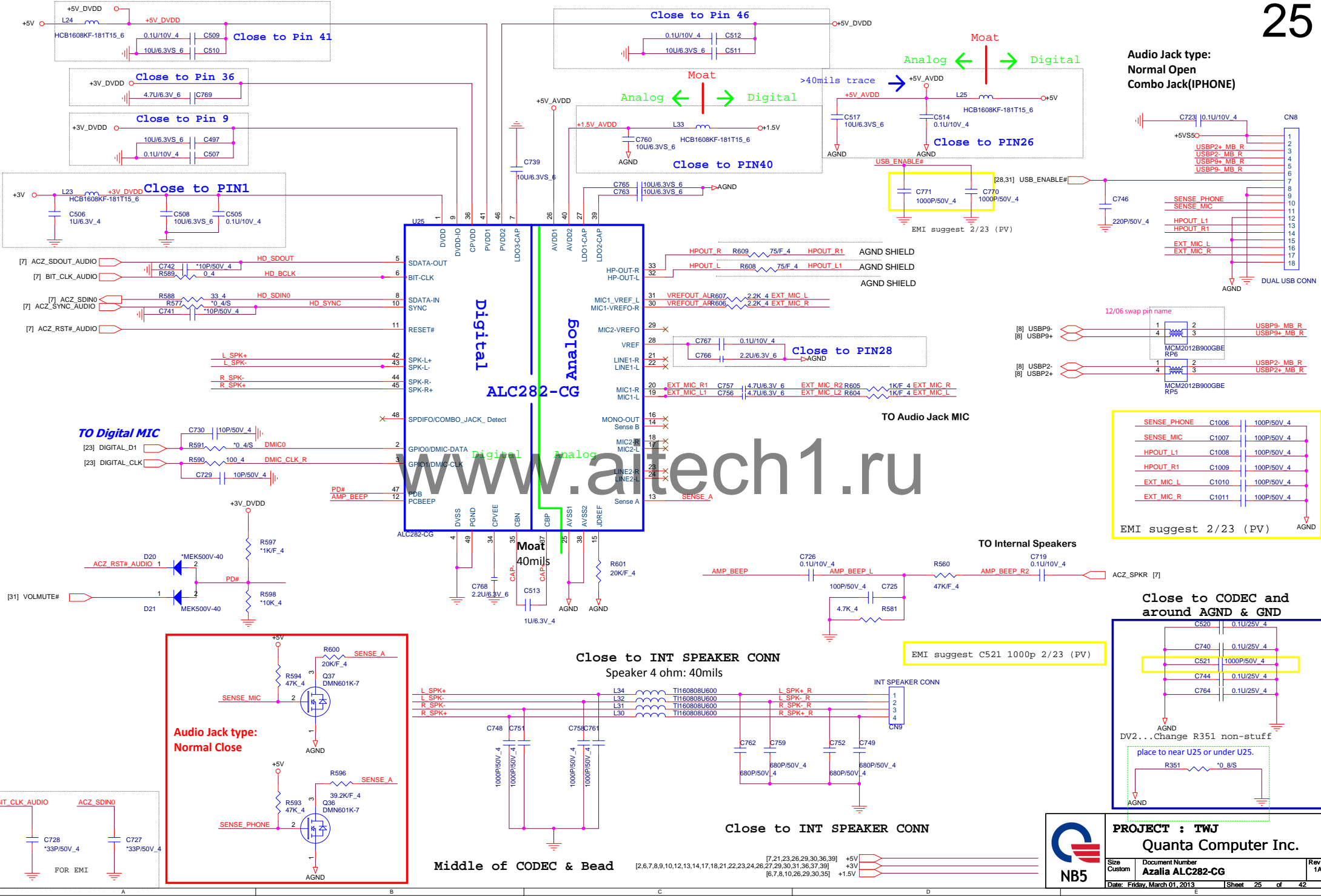


PROJECT : TWJ  
Quanta Computer Inc.

Size	Document Number
Custom	<b>RT65237 8 GB SOCKET</b>

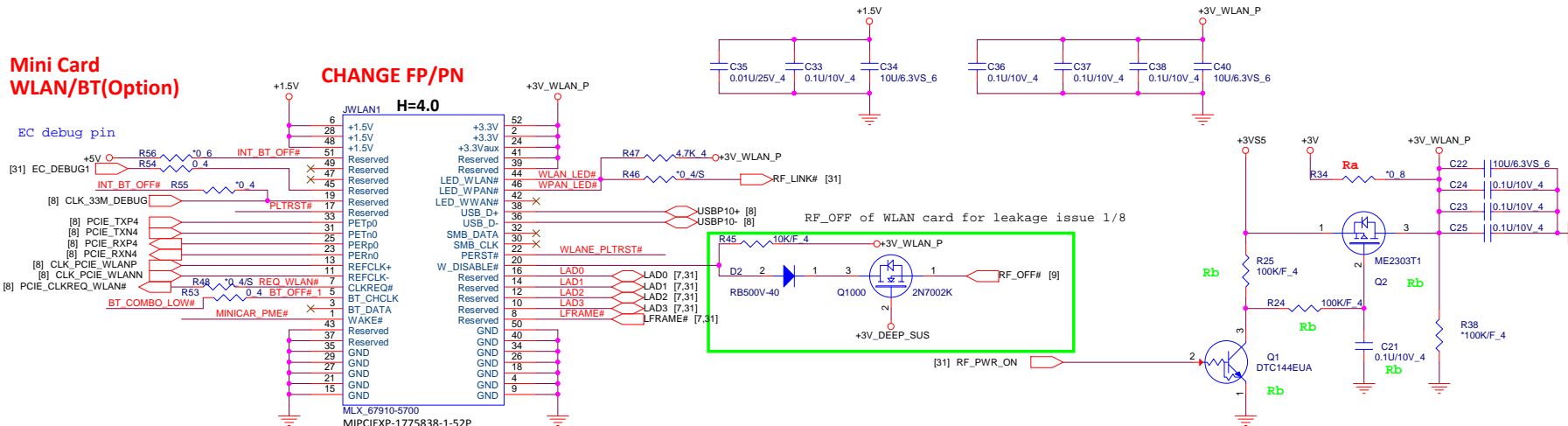
Rev  
1A





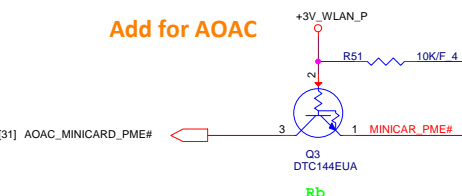
**Mini Card  
WLAN/BT(Optional)**

EC debug pin

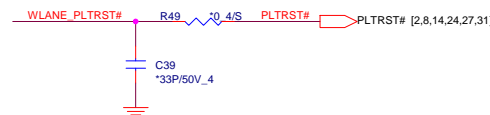


### Support Wake Function(Reserve)

Add for AOAC

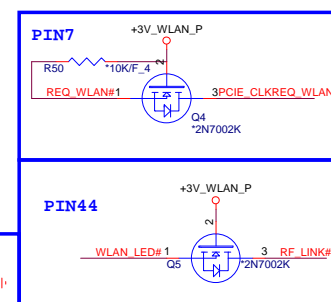


## Mini Card Reset



non-AOAC	LG	Ra
AOAC	CB	Rb

Avoid leakage issue

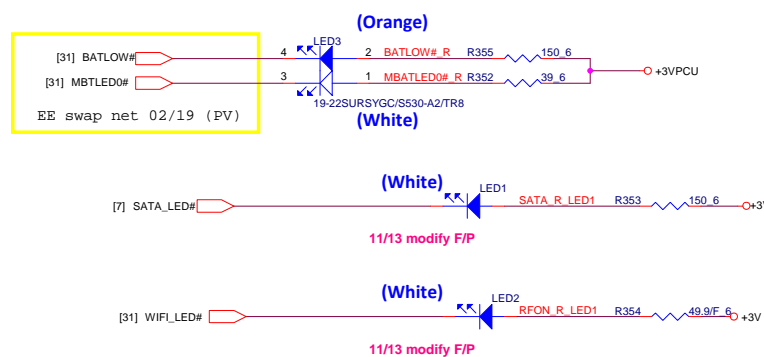


For EMI Suggestion

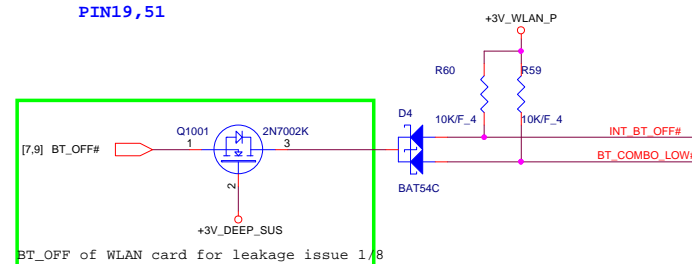


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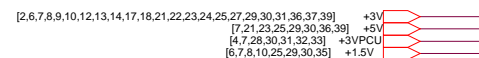
## LED Status



## PIN19,51



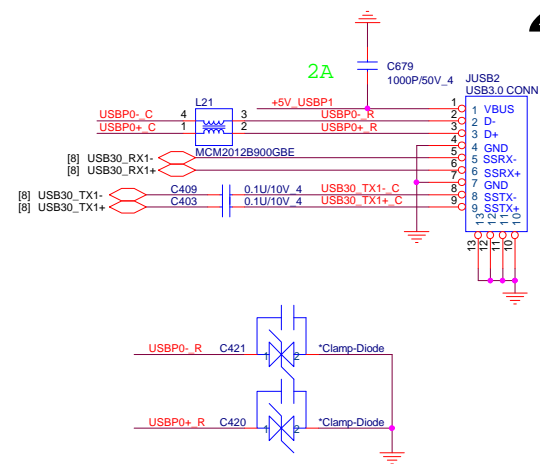
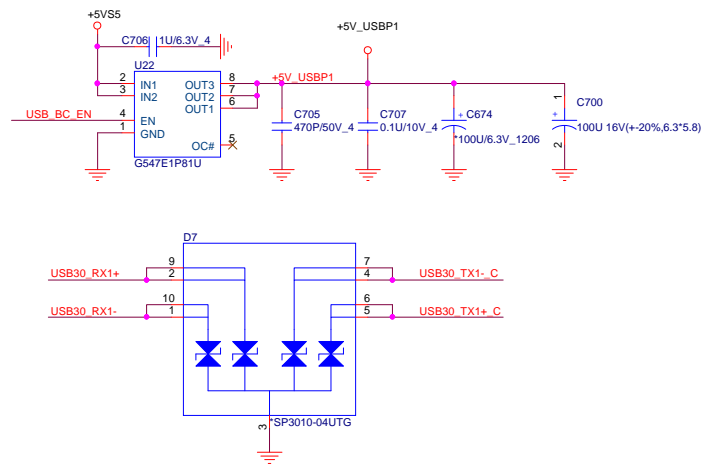
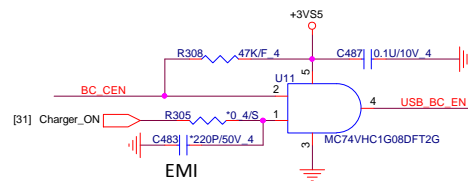
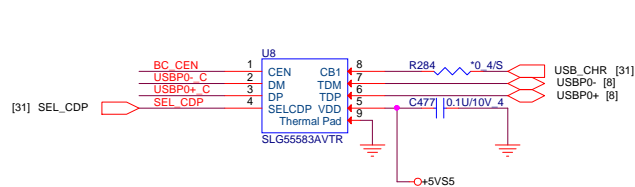
9/4 Intel COMBO card control circuit  
1.add R1001,R1002,Q1001  
2.add net name"INT BT COMBO EN#" -> "INT BT OFF#"





# Charge USB/USB3.0 COMBO X1

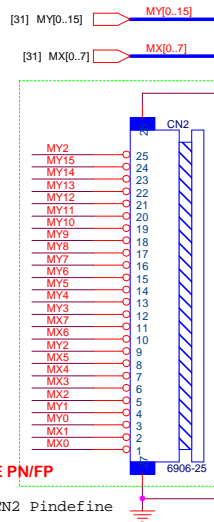
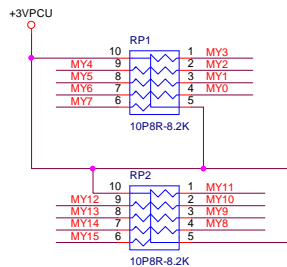
28



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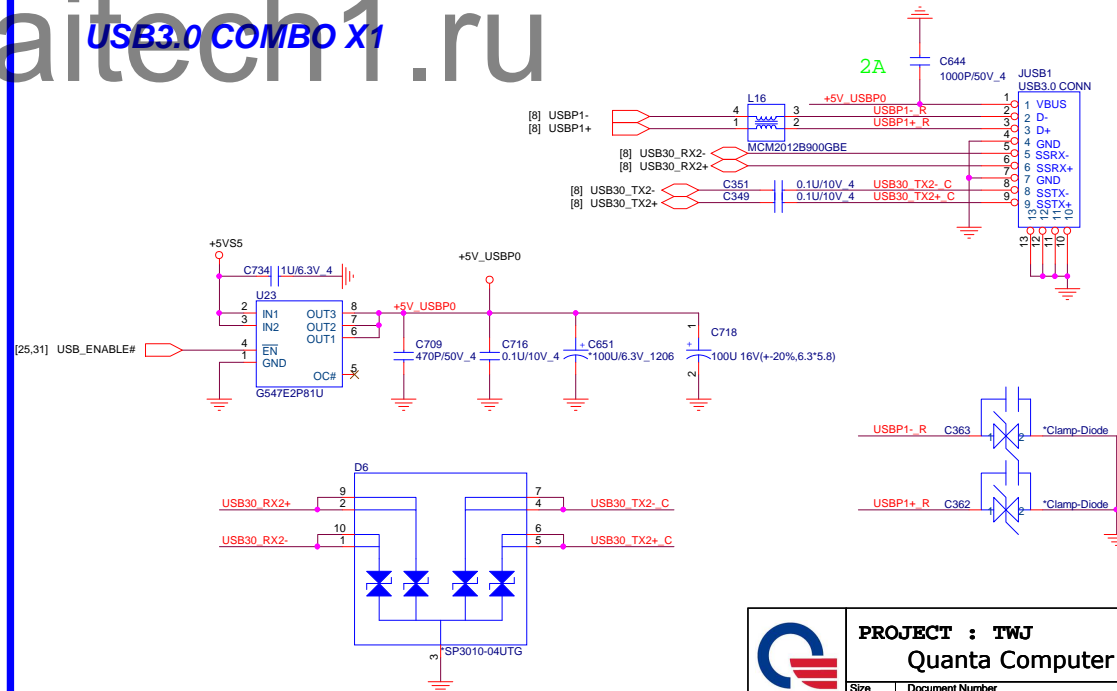
USB3.0 COMBO X1

## Keyboard Connector



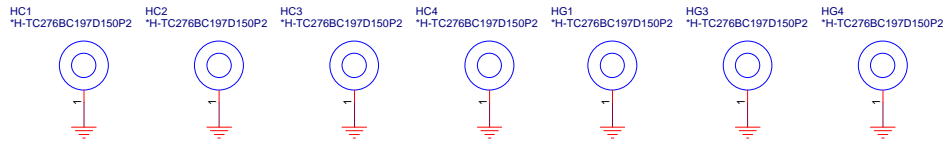
CHANGE PN/FP  
DV2...Change CN2 Pindefine

MY1	C109	220P/50V_4
MY2	C113	220P/50V_4
MY3	C101	220P/50V_4
MY4	C101	220P/50V_4
MY5	C100	220P/50V_4
MY6	C99	220P/50V_4
MY7	C98	220P/50V_4
MY8	C97	220P/50V_4
MY9	C96	220P/50V_4
MY10	C95	220P/50V_4
MY11	C94	220P/50V_4
MY12	C93	220P/50V_4
MY13	C116	220P/50V_4
MY14	C115	220P/50V_4
MY15	C114	220P/50V_4

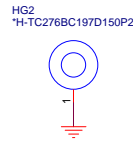


NB5	PROJECT : TWJ		
	Quanta Computer Inc.		
Size	Document Number	Rev	
Custom	USB3.0/Charge USB/KBD/	1A	
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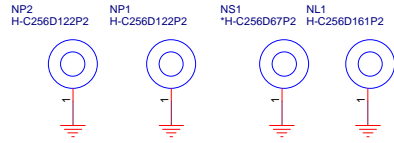
## CPU Bracket



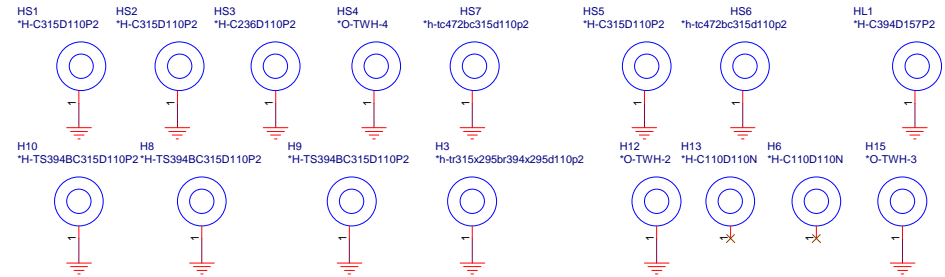
## GPU Bracket



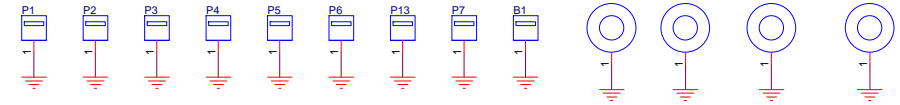
## PCH NU Screw Hold



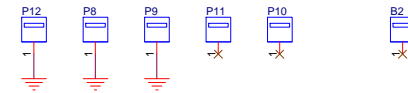
## System Screw Hold



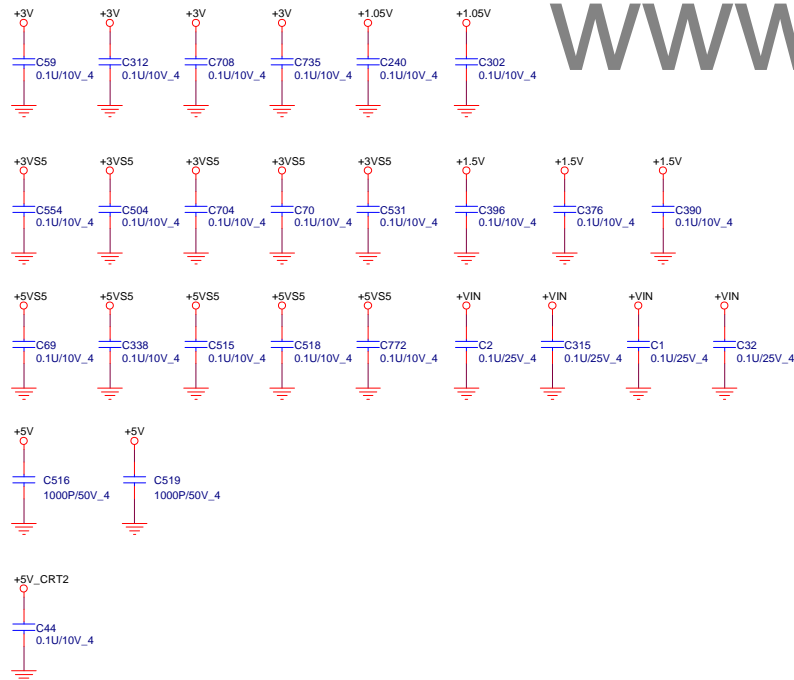
## System Pad(Top)



## System Pad(Button)



## EMI CAP



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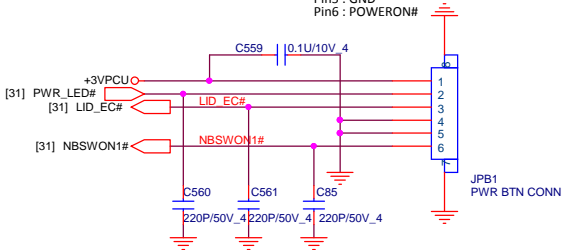
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,27,30,31,36,37,39]	+3V
[25,28,33,34,35,36,37,38,39,40]	+5VS5
[2,6,7,9,10,26,28,31,33,35,36,41]	+3VS5
[23,32,33,34,35,37,39,40,41]	+VIN
[2,4,7,9,10,34,41]	+5V CRT2
[7,21,23,25,26,30,36,39]	+1.05V
[6,7,8,10,25,26,30,35]	+5V
	+1.5V

NB5	PROJECT : TWJ		
	Quanta Computer Inc.		
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	Hole / EMI Cap		
Date: Friday, March 01, 2013	Sheet 29 of 42		

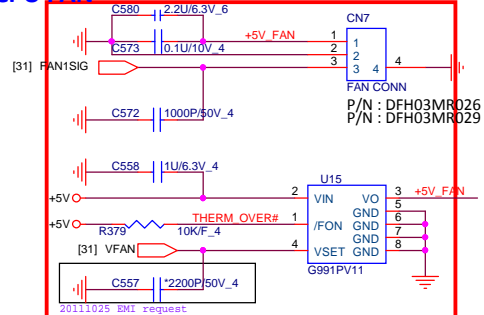


## Power Button Connector

Pin1 : +3VPCU(LIDSWITCH PWR)  
Pin2 : POWER LED  
Pin3 : LIDSWITCH  
Pin4 : GND  
Pin5 : GND  
Pin6 : POWERON#

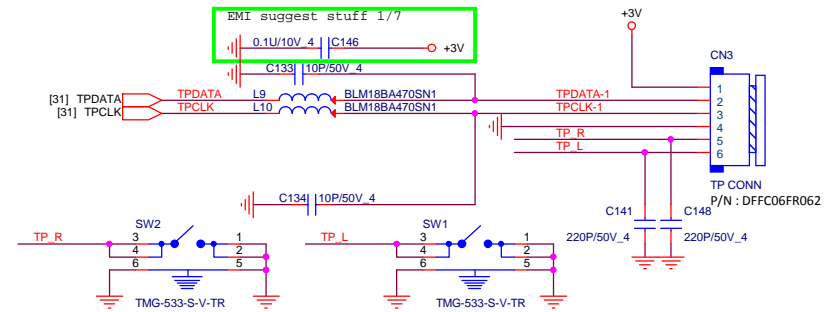


## CPU FAN

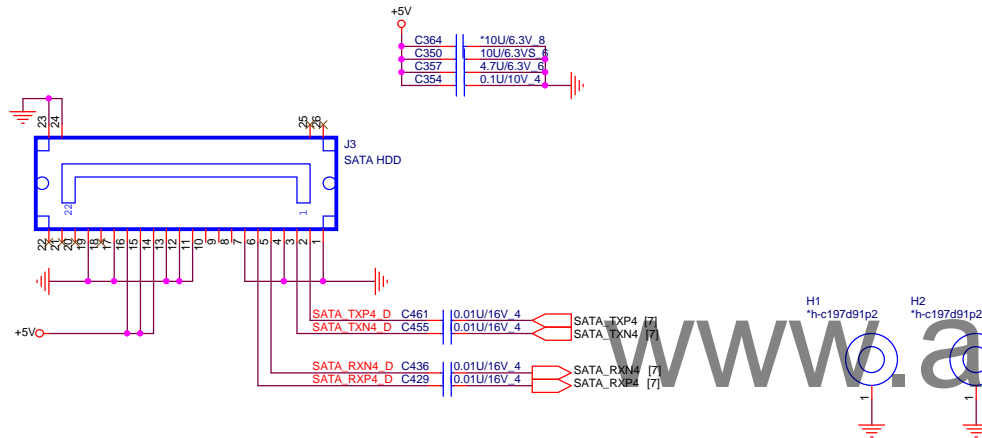


## Touch Pad Connector

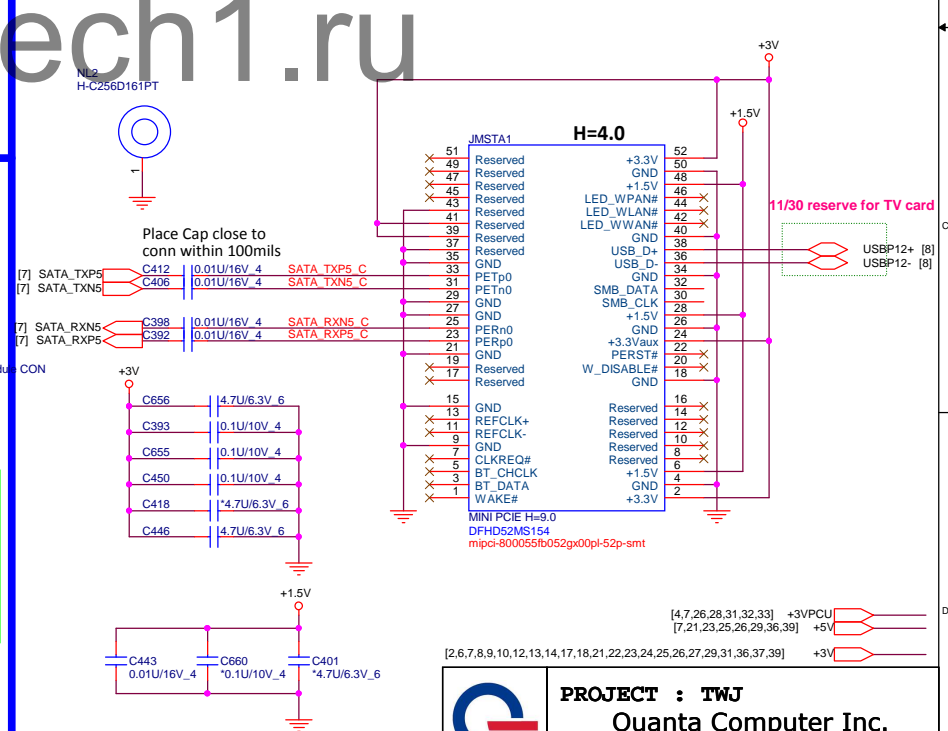
B-stage change footprint to 88513-0601-6p-l-smt



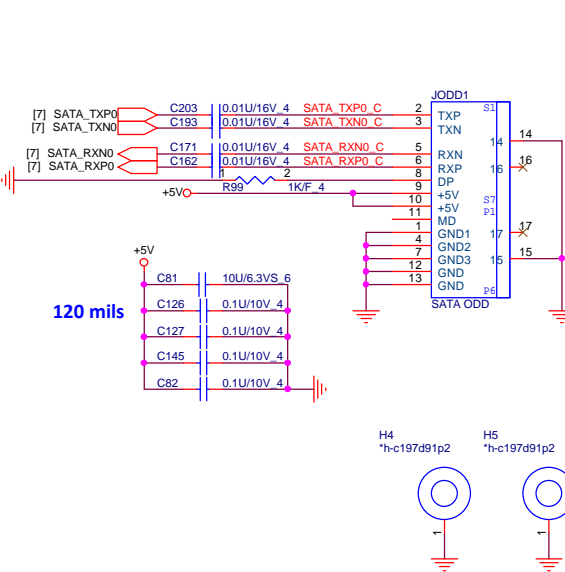
## SATA HDD CONNECTOR



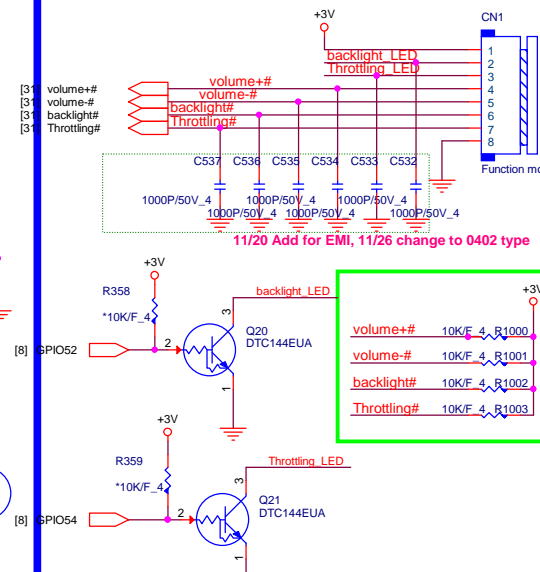
## MINISATA



## SATA ODD Connector



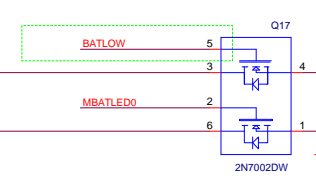
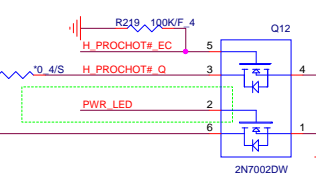
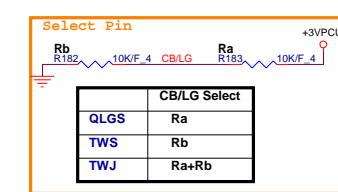
## Function Module connector



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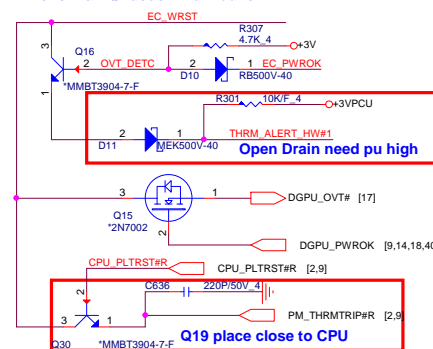
Size Custom Document Number SW/TP/FAN/HDD/ODD/mSATA Rev 1A

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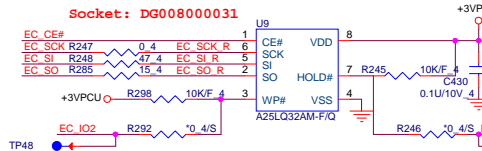


TPCLK R228 10K/F 4  
 TPDATA R233 10K/F 4  
 MBCLK2 R260 10K/F 4  
 MBDATA2 R261 10K/F 4

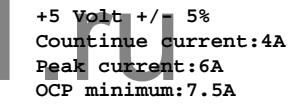
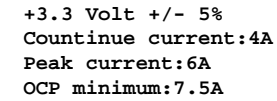
stuff R228,R233 for touch pad  
 function 1/7

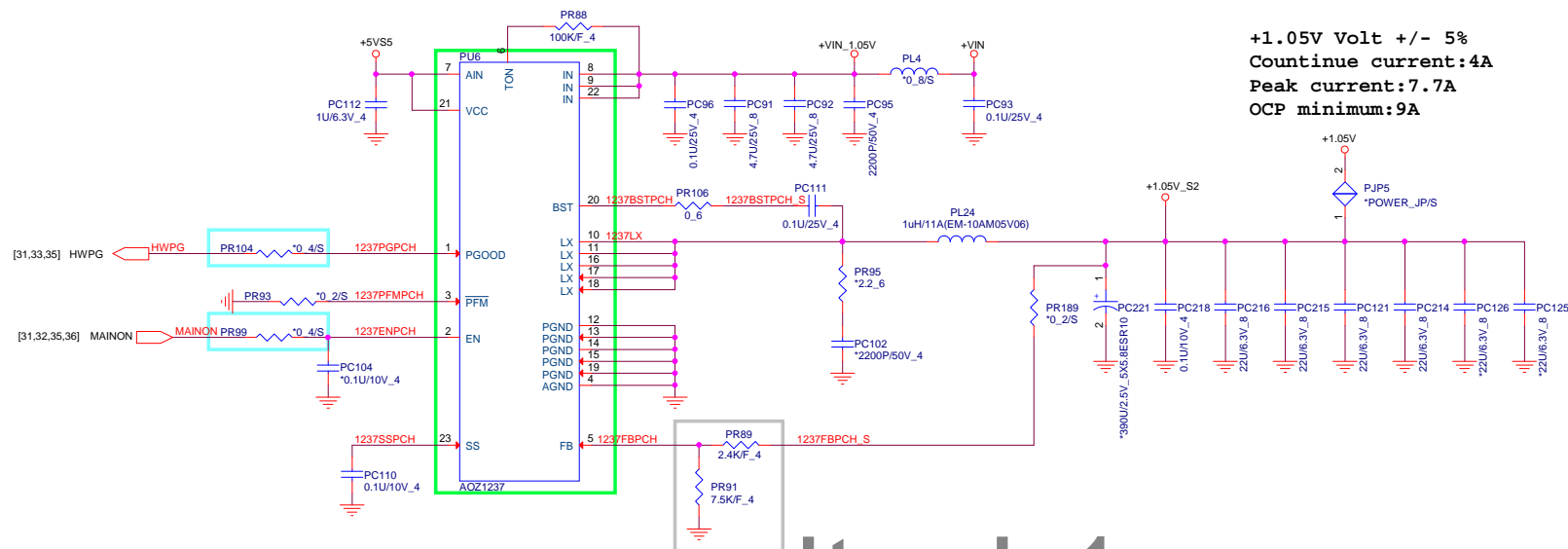


Socket: DG008000031






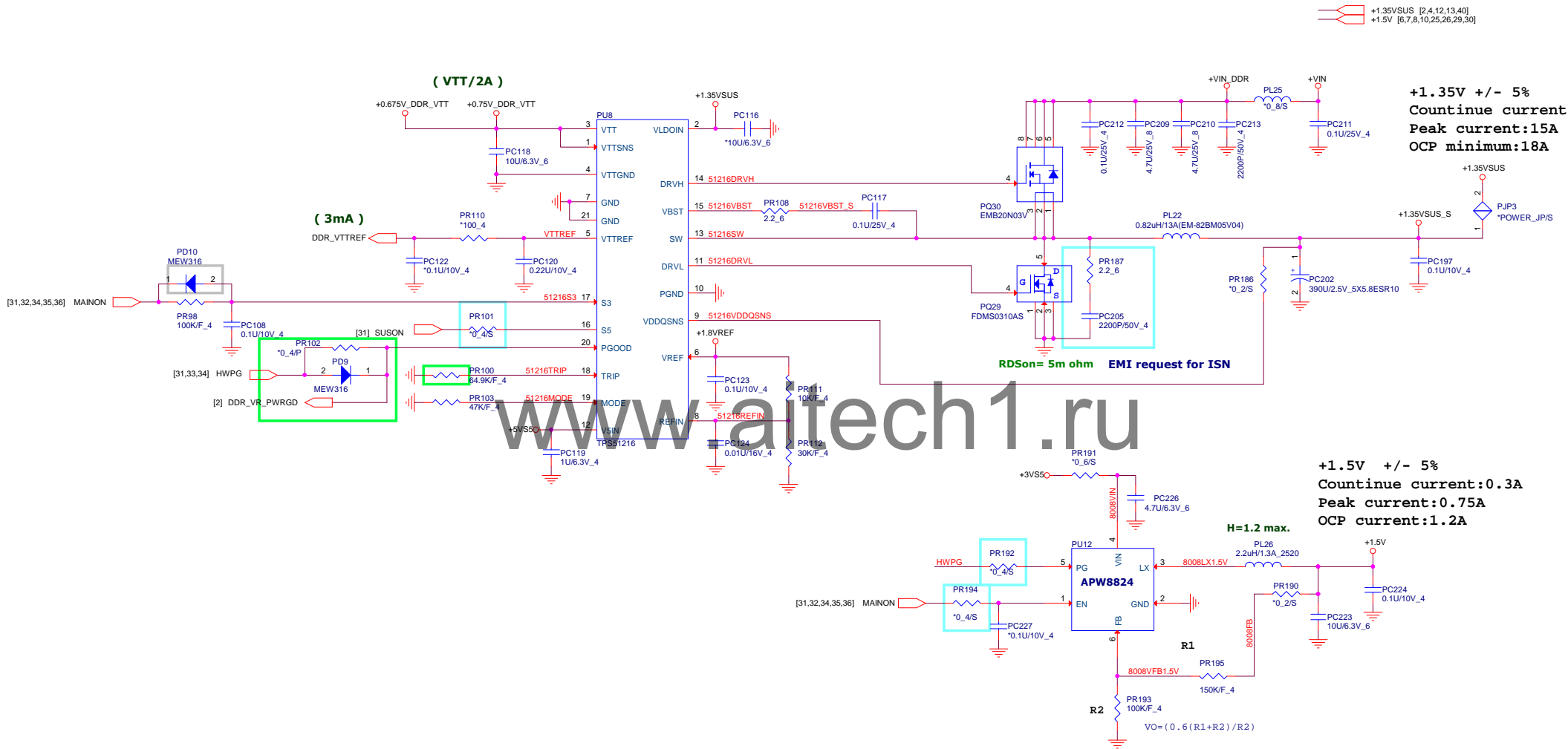




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+1.05V [2,4,7,9,10,29,41]

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	Quanta Computer Inc.	
Size	Document Number	Rev
Custom	1.05V(RT8228BZ)	1A
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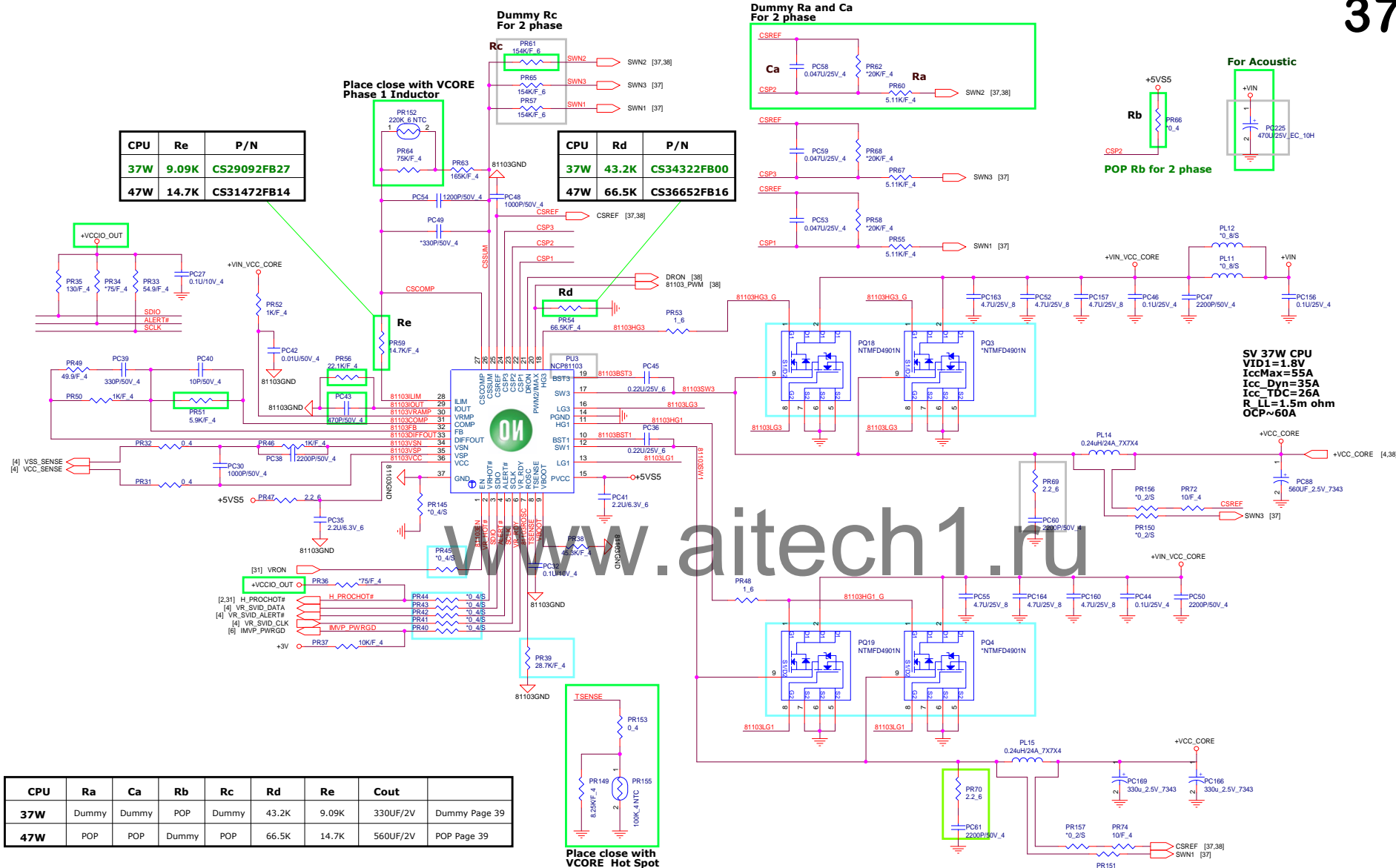




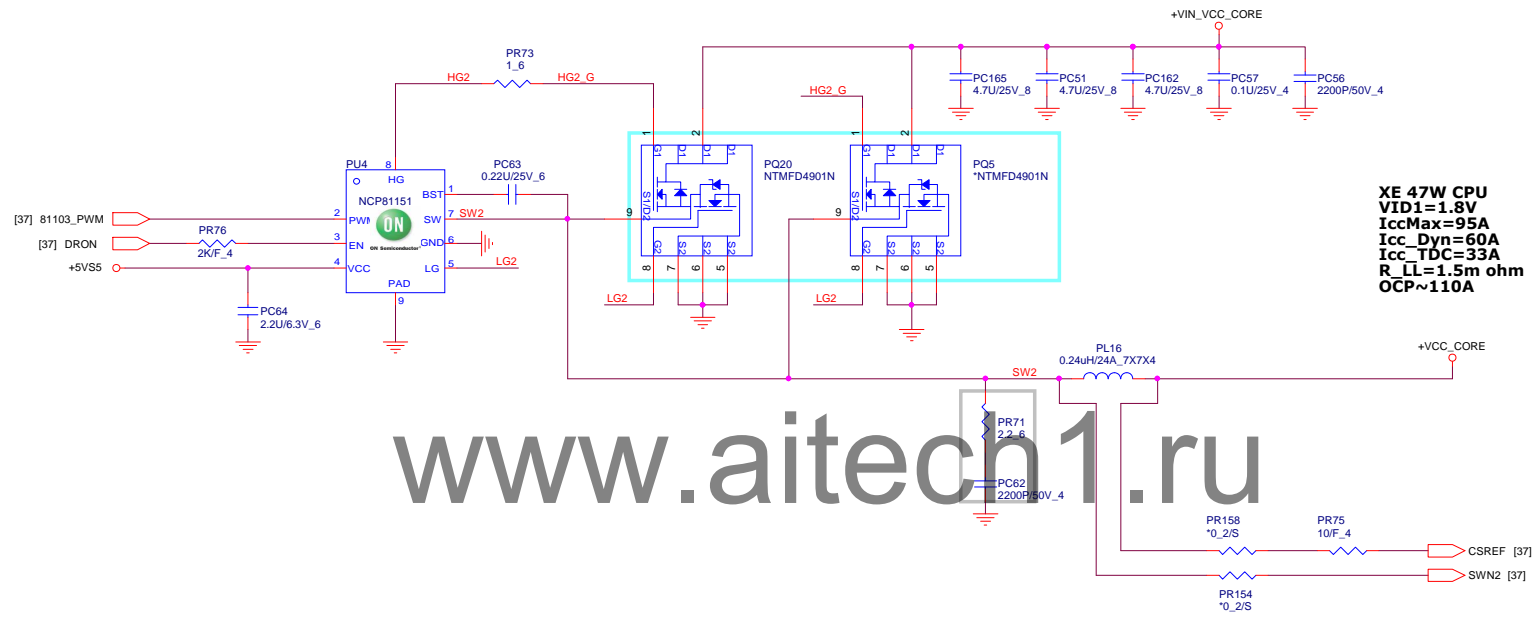


CPU	Re	P/N
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14


CPU	Rd	P/N
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

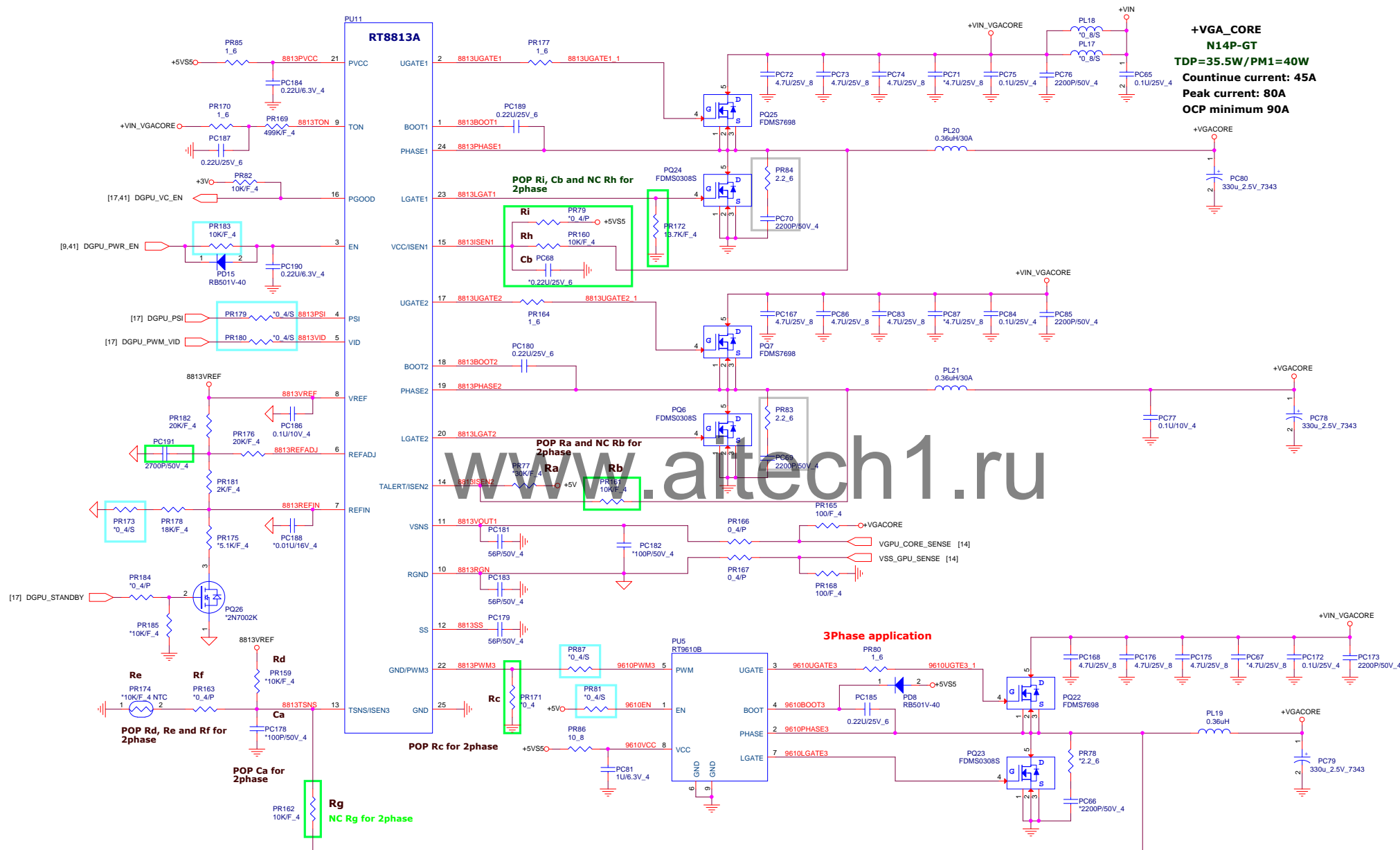


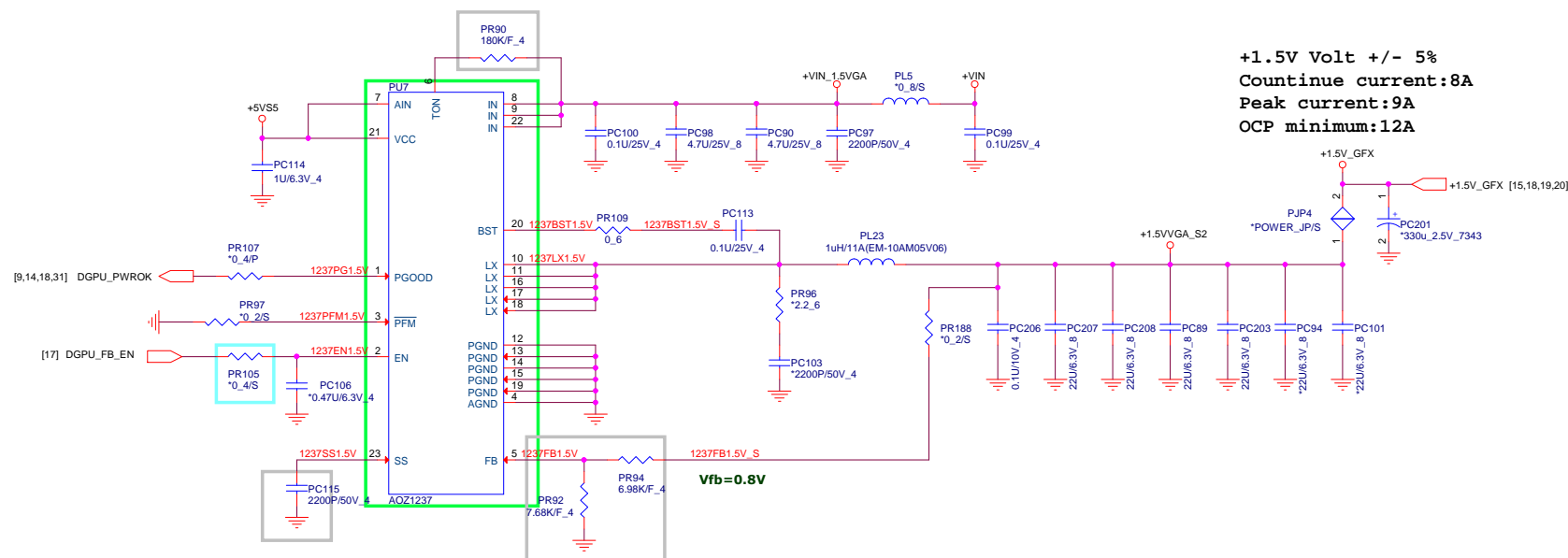
CPU	Ra	Ca	Rb	Rc	Rd	Re	Cout	
37W	Dummy	Dummy	POP	Dummy	43.2K	9.09K	330UF/2V	Dummy Page 39
47W	POP	POP	Dummy	POP	66.5K	14.7K	560UF/2V	POP Page 39



+VCC\_CORE [4,37]

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